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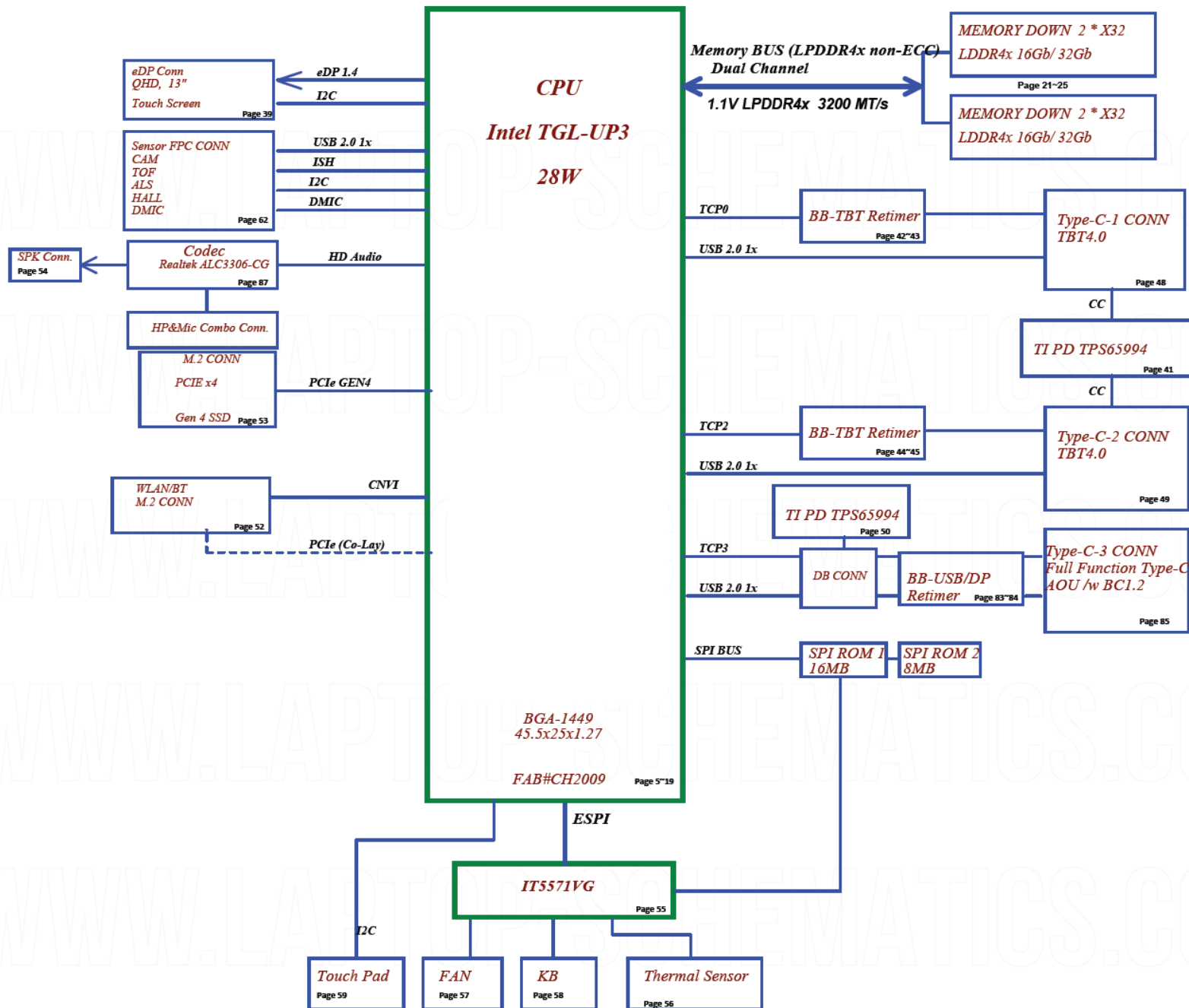
S750-13_NB2608_MB&DB Schematics Document

Intel TGL Lake UP3-Processor with LPDDR4x MD

REV4.0

2020-07-27

Author	Zhengxingxing & Ouyangqindan	 HUAQIN 华勤通信 Huaqin Telecom Technology Com.,Ltd.		
Reviewer	Zhangshaodi & Weilantao	Page name: Cover page		
Approver	Leizhao_Hai	Size: A4	Project Name: S750-13/NB2608	REV: V4.0
		Date: Friday, July 31, 2020	Sheet: 1	of 90



MEM ID

HW_ID0	HW_ID1	HW_ID2	HW_ID3	Description	Total
0	0	0	0	4x Samsung 16Gb K4U6E3S4AA-MGCR	8GB
1	0	0	0	4x Micron 16Gb MT53E512M32D2NP-046 WT:E	8GB
0	1	0	0	4x Hynix 16Gb H9HCNNNBKMLHR-NEE	8GB
0	0	1	0	CHA: 2x Samsung 16Gb K4U6E3S4AA-MGCR CHB: 2x Samsung 32Gb K4UBE3D4AA-MGCR	CHA:4GB CHB:8GB Total 12GB
0	0	0	1	CHA: 2x Micron 16Gb MT53E512M32D2NP-046 WT:E CHB: 2x Micron 32Gb MT53E1G32D2NP-046 WT:A	CHA:4GB CHB:8GB Total 12GB
1	1	0	0	CHA: 2x Hynix 16Gb H9HCNNNBKMLHR-NEE CHB: 2x Hynix 32Gb H9HCNNNCPMBLHR-NEE	CHA:4GB CHB:8GB Total 12GB
0	1	1	0	4x Samsung 32Gb K4UBE3D4AA-MGCR	16GB
0	0	1	1	4x Micron 32Gb MT53E1G32D2NP-046 WT:A	16GB
1	1	1	0	4x Hynix 32Gb H9HCNNNCPMBLHR-NEE	16GB

Phase ID

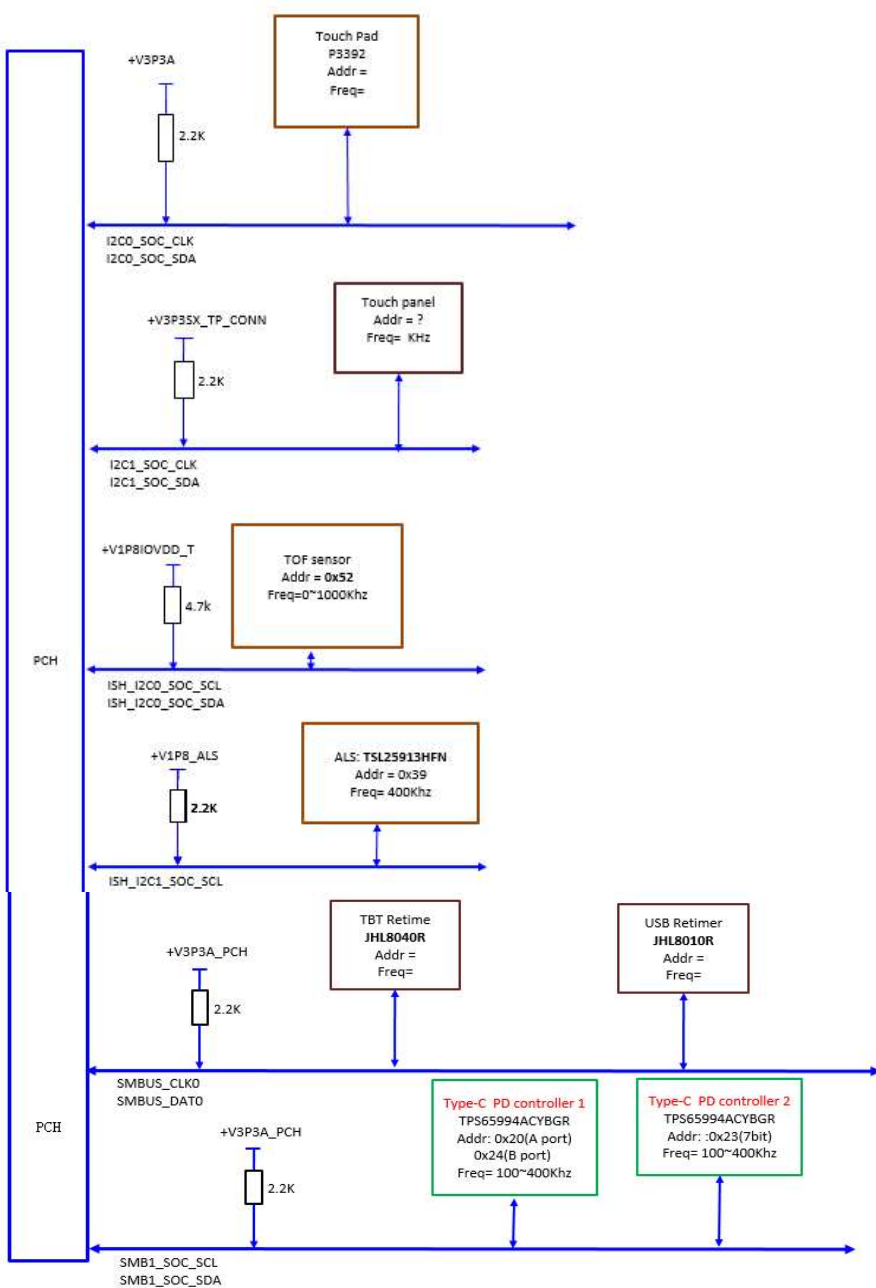
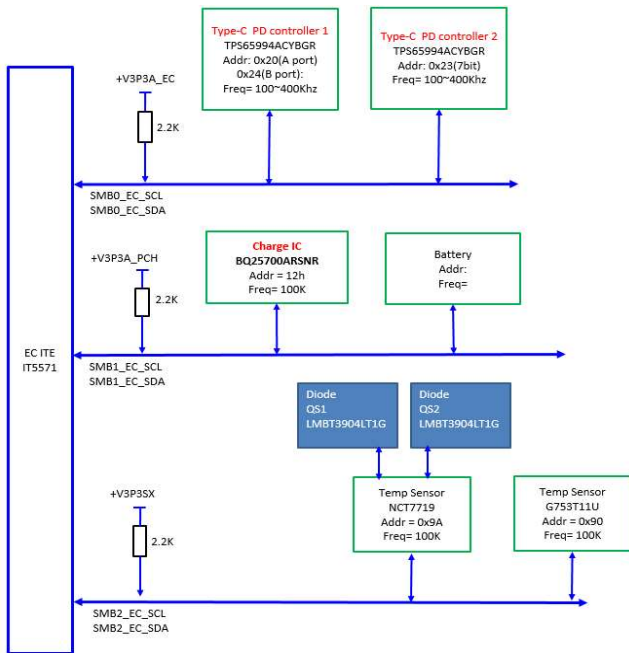
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0	0	EVT
1	0	FVT
0	1	SIT
1	1	SVT

Project ID

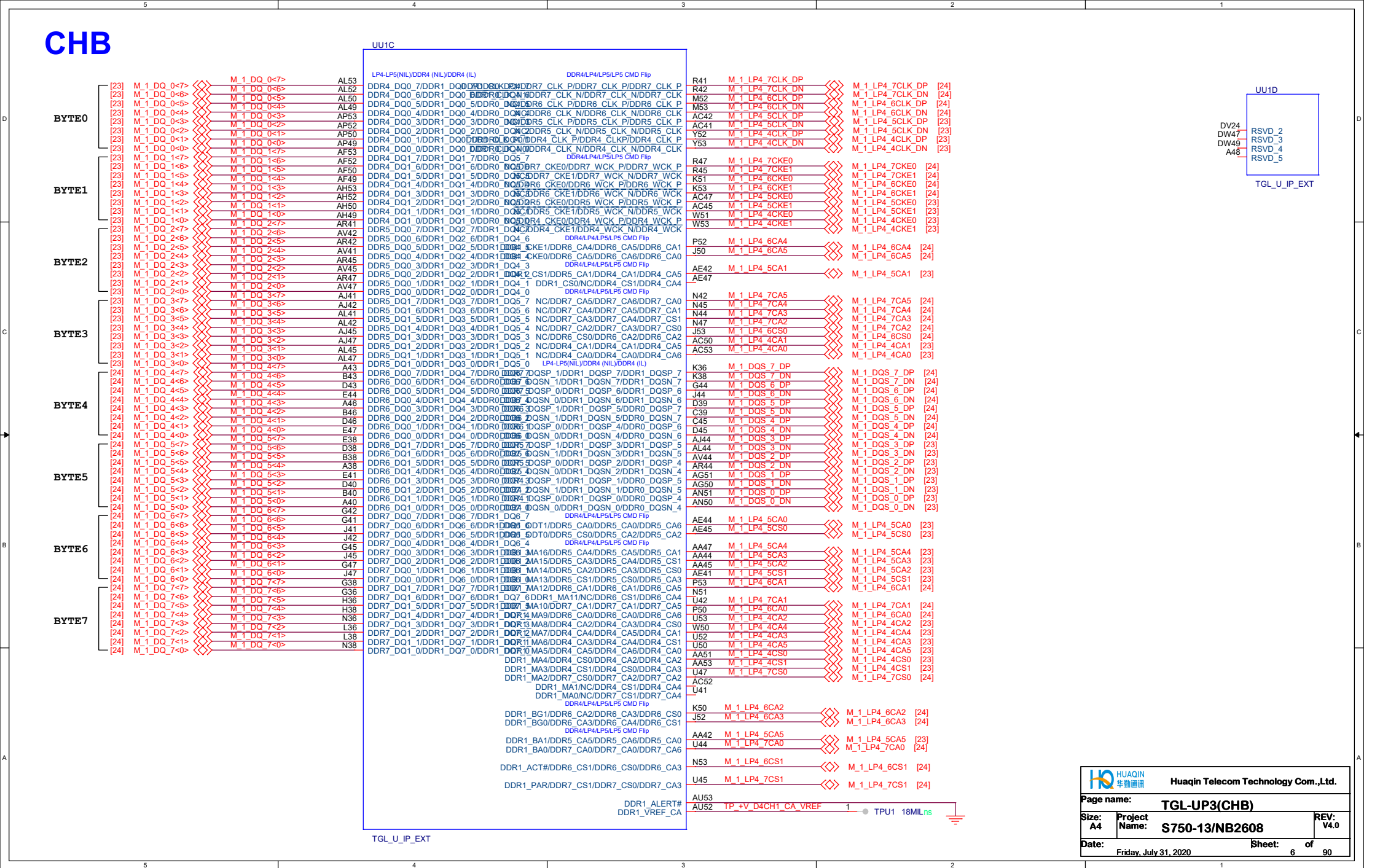
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1	NB2609

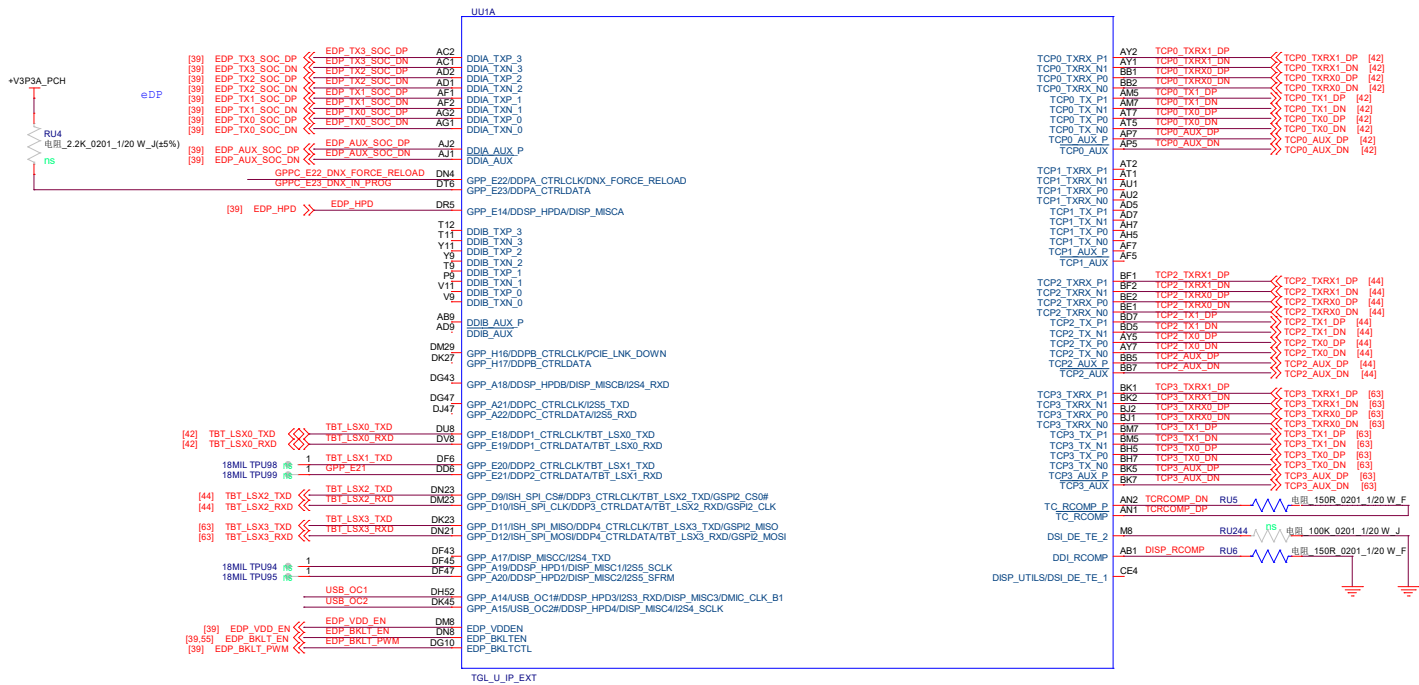
Reserve ID

HW_ID7	Description
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1	Reserve



CHB



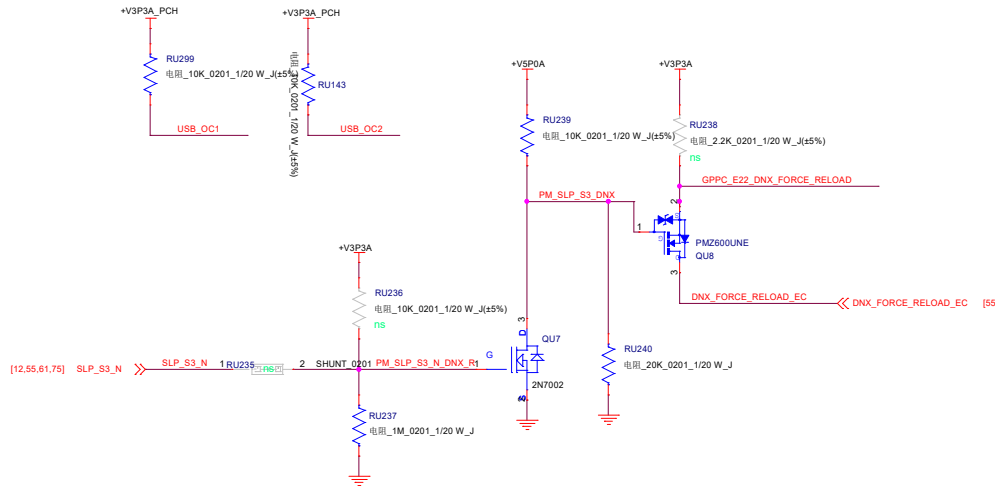
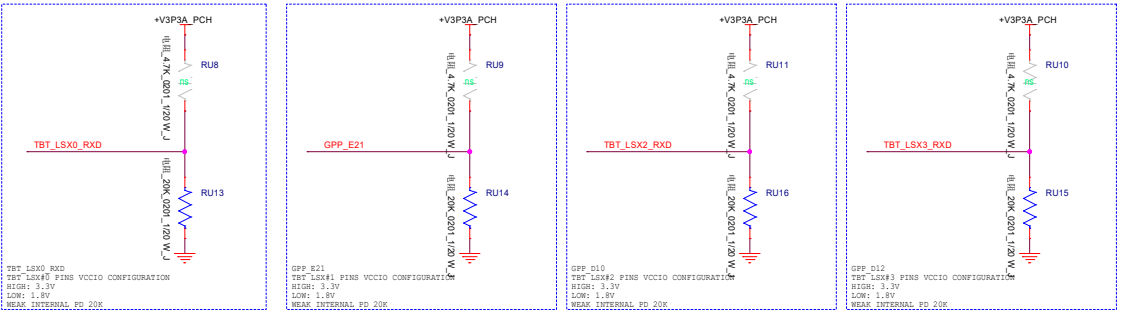


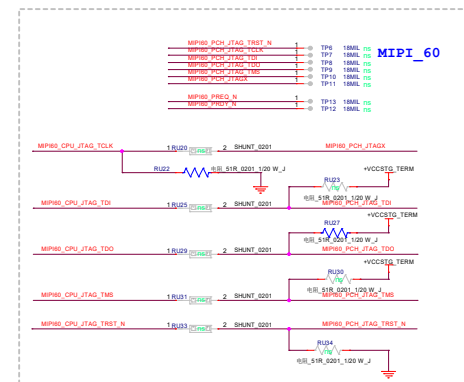
TBT_1

TBT_2

Type-C_3

PCH STRAP---VCCIO CONFIGURATION



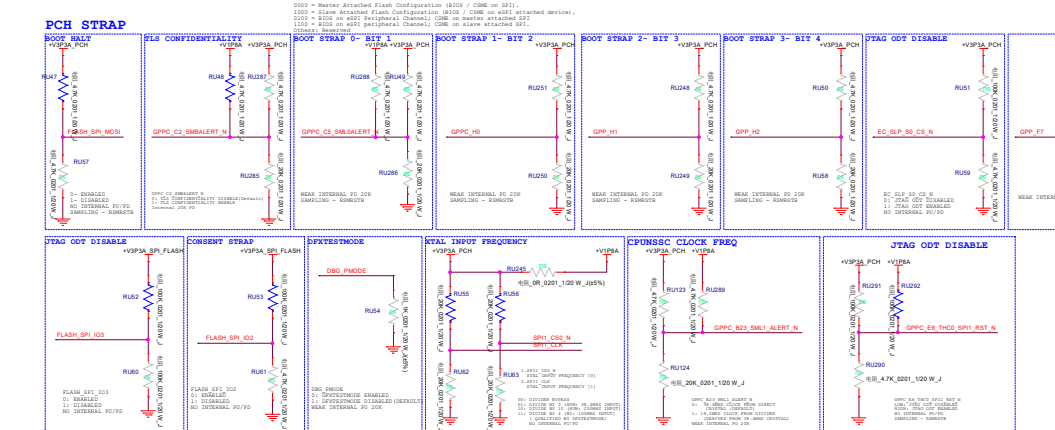
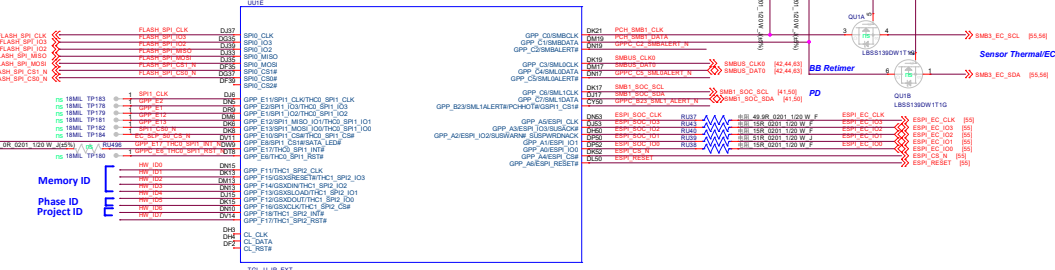
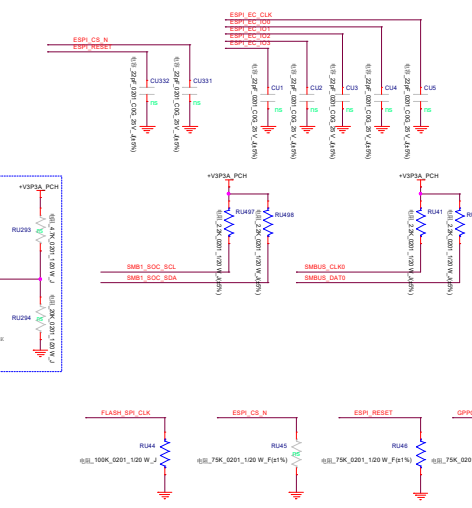


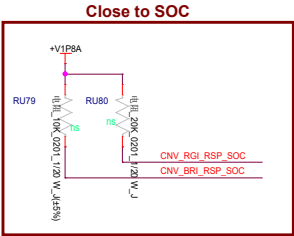
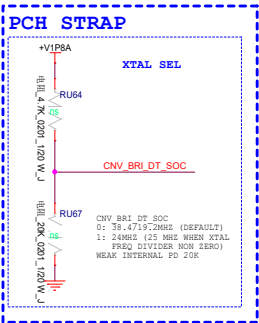
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0	0	0	0	4a Hexagon 1600: X400E3AAA-MC0A	602B
0	0	0	0	4a Micron 1600: M753E126232020-046 WT-E	602B
0	1	0	0	4a Nynix 1600: H99C00000000-046-HEE	602B
1	0	1	1	4a Hexagon 1600: X400E3AAA-MC0A	602B (120B)
0	0	0	1	4a Micron 1600: M753E126232020-046 WT-E	602B (120B)
0	0	0	1	4a Nynix 1600: H99C00000000-046-HEE	602B (120B)
1	1	1	1	4a Hexagon 1600: X400E3AAA-MC0A	602B (120B)
0	0	0	1	4a Micron 1600: M753E126232020-046 WT-E	602B (120B)
0	0	0	1	4a Nynix 1600: H99C00000000-046-HEE	602B (120B)
0	0	0	1	4a Hexagon 1600: X400E3AAA-MC0A	602B (120B)
0	0	0	1	4a Micron 1600: M753E126232020-046 WT-E	602B (120B)
0	0	0	1	4a Nynix 1600: H99C00000000-046-HEE	602B (120B)

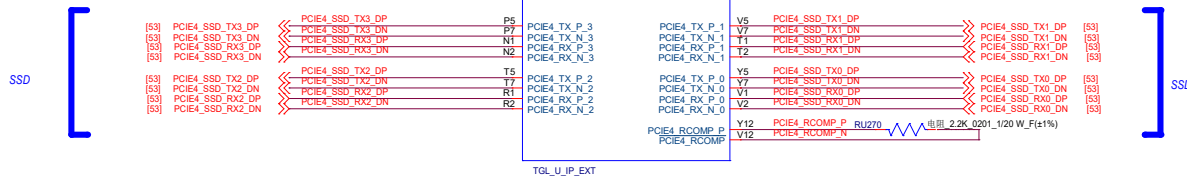
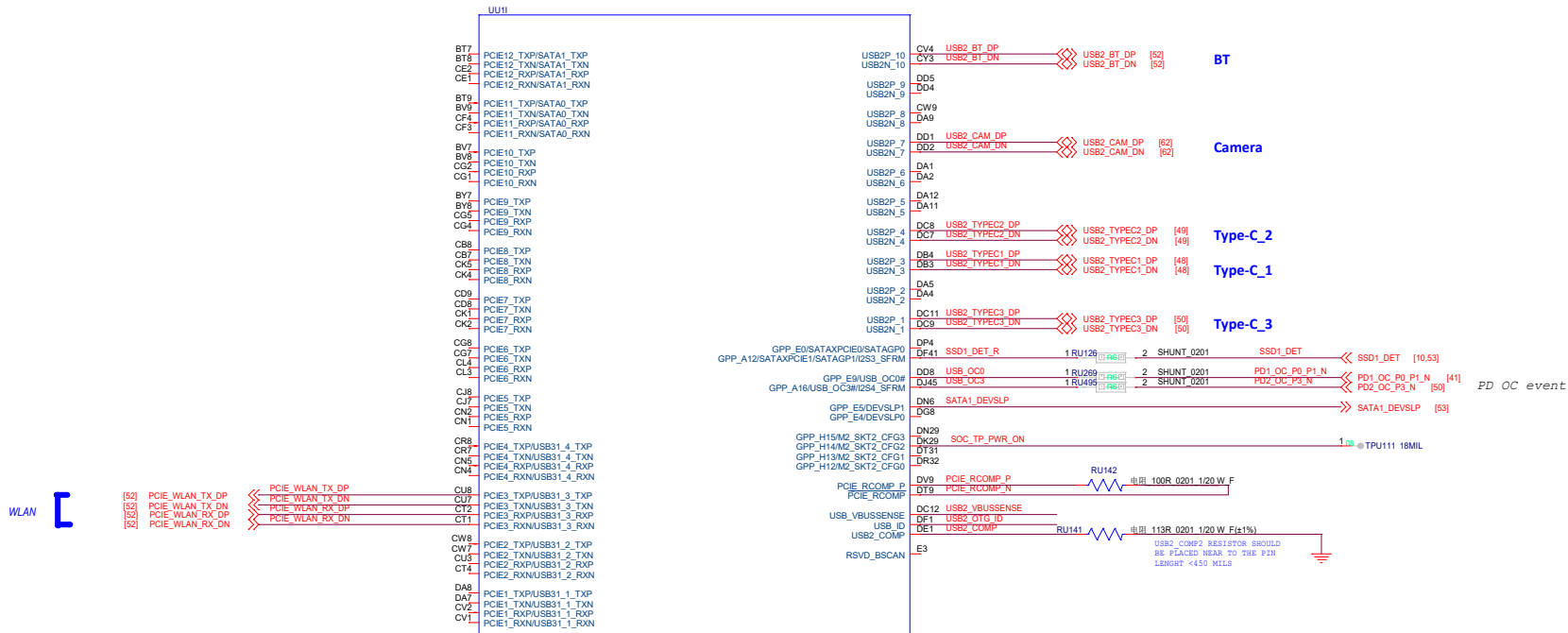
Phase ID

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1	0	SVT
0	1	SIV
1	1	SVT

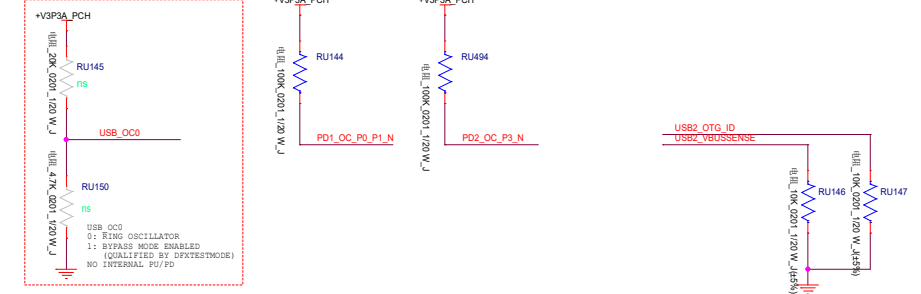
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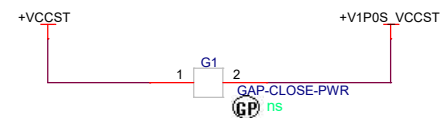
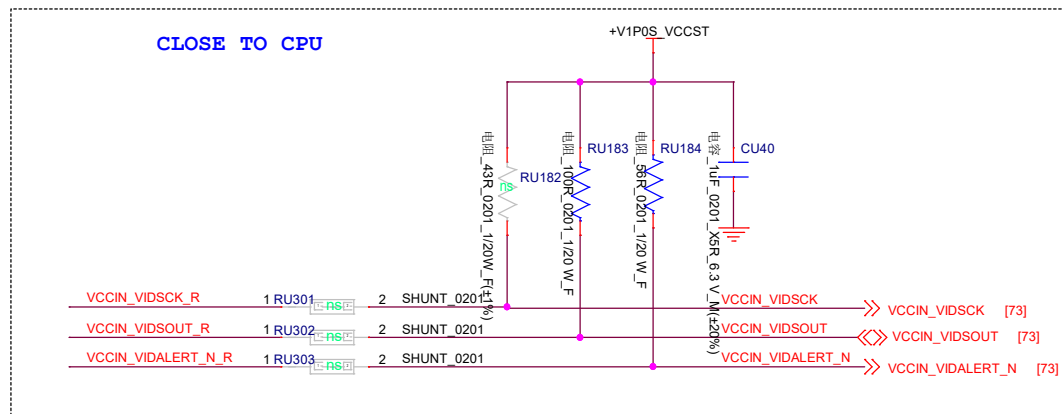
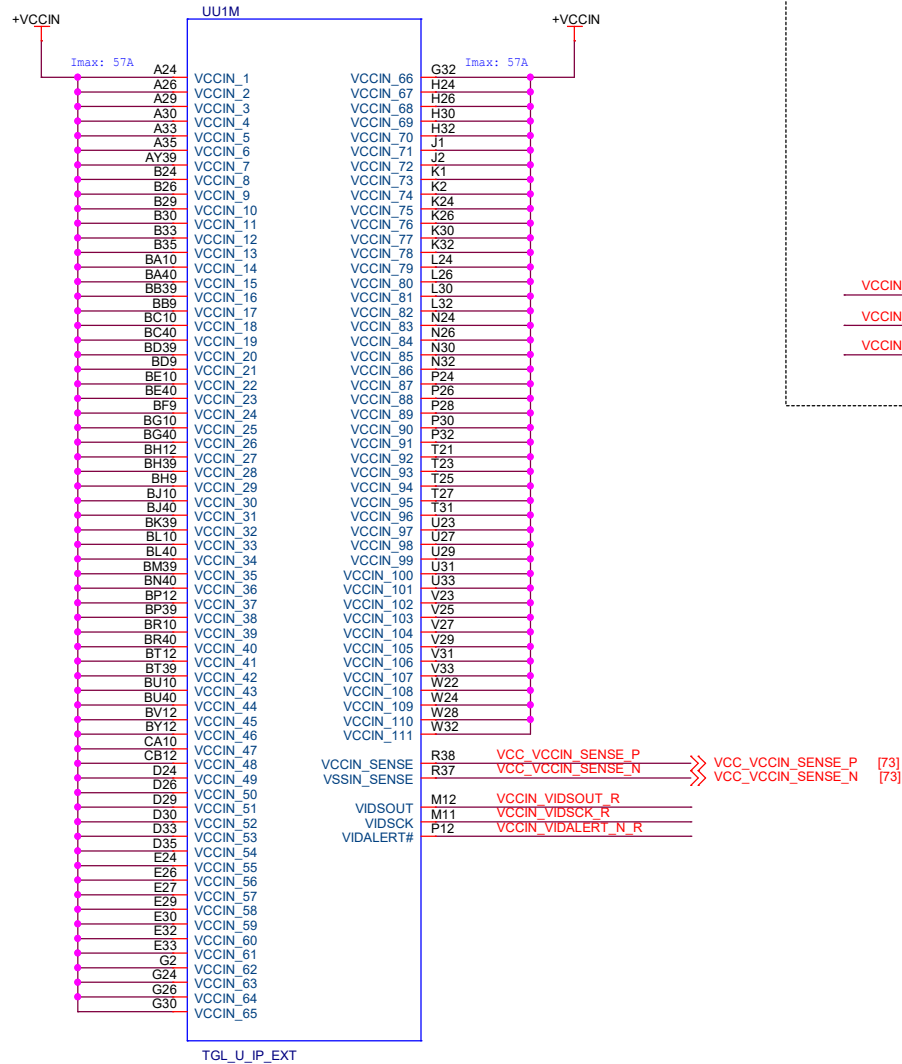


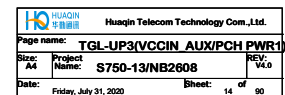


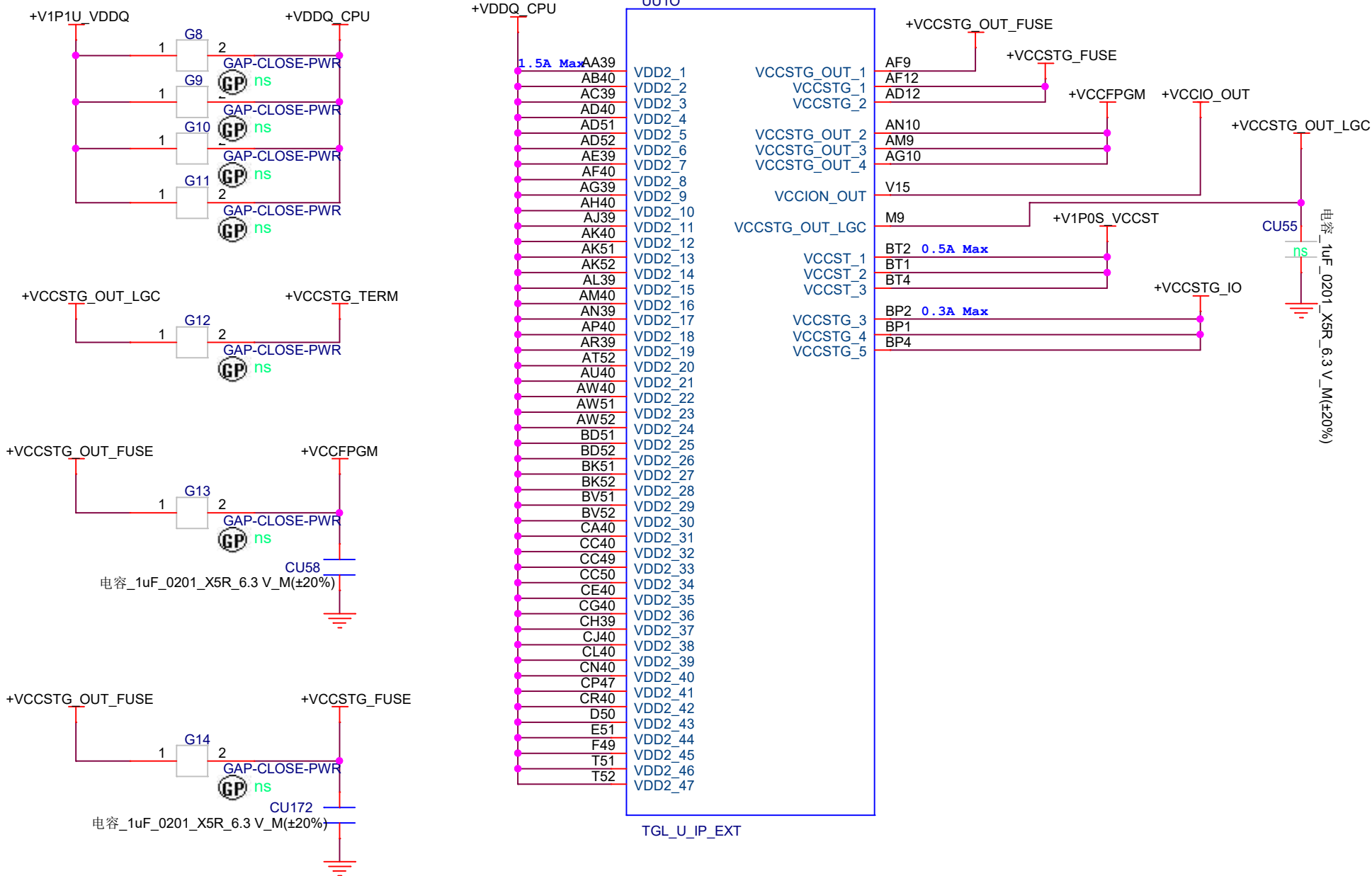


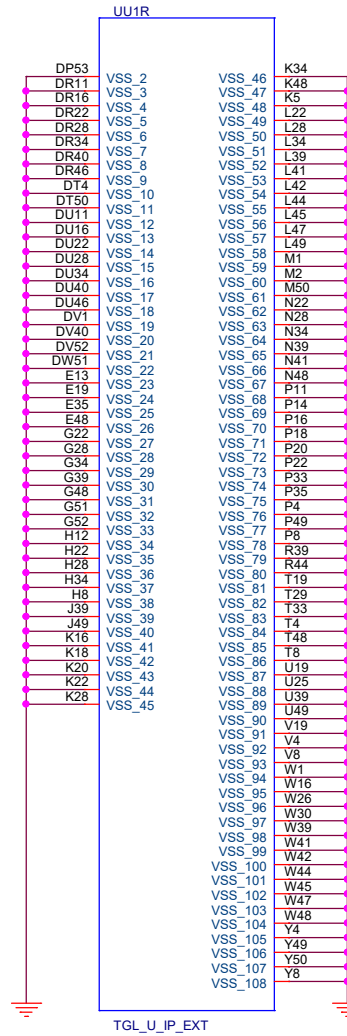
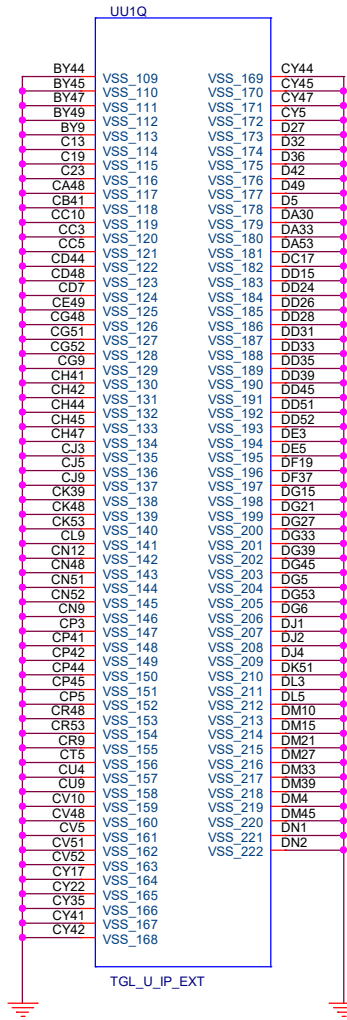
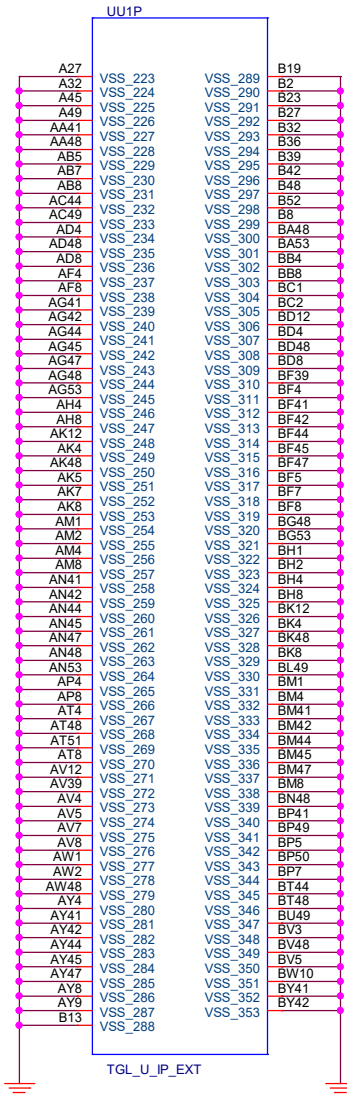
PCH STRAP

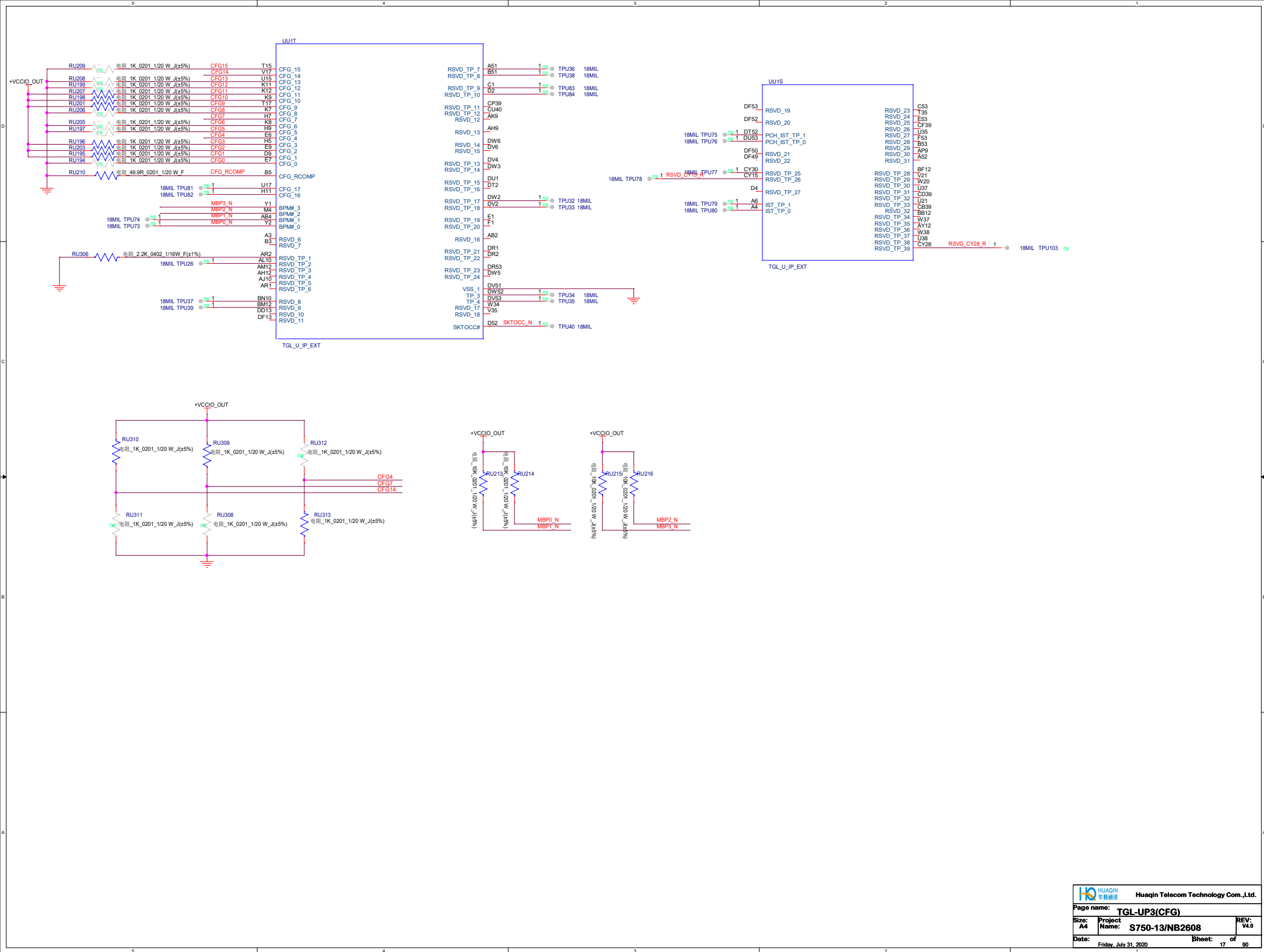


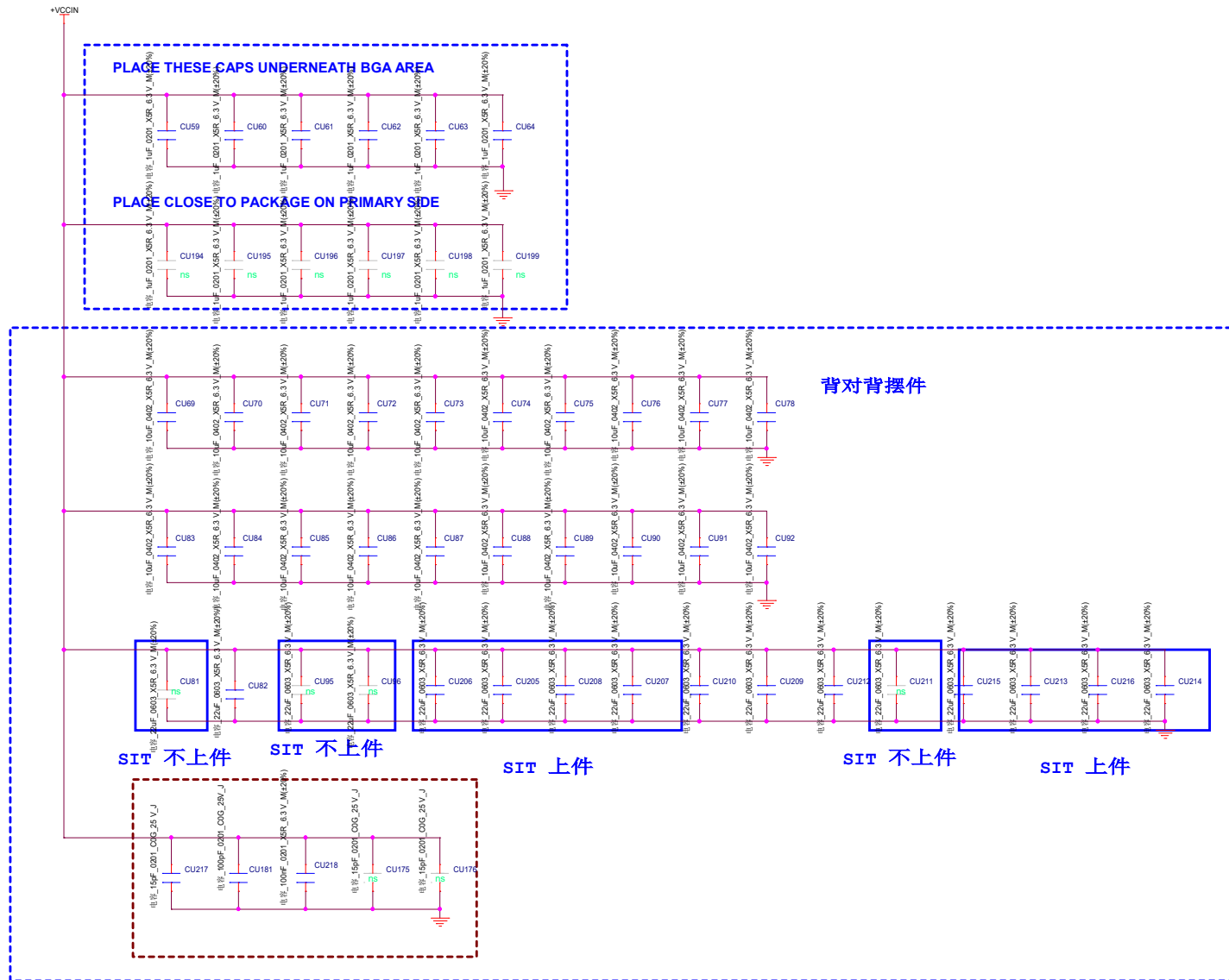




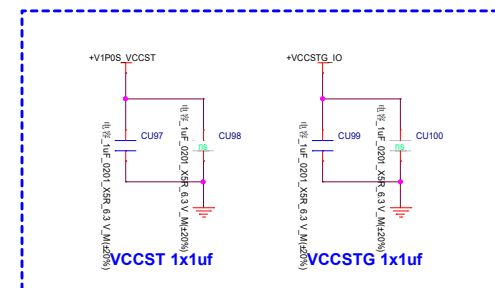






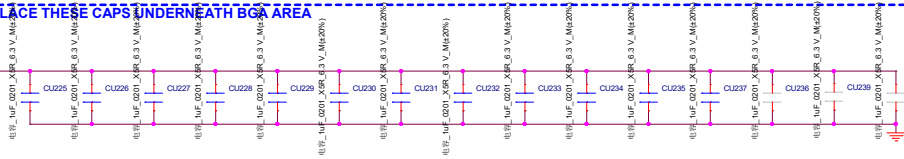


+VCCIN			
	PDG	NB2608	
1uF	12	6(NC)+6	
10uF	12	20	
22uF	10	12+4(NC)	
47uF			
220uF	4	2	

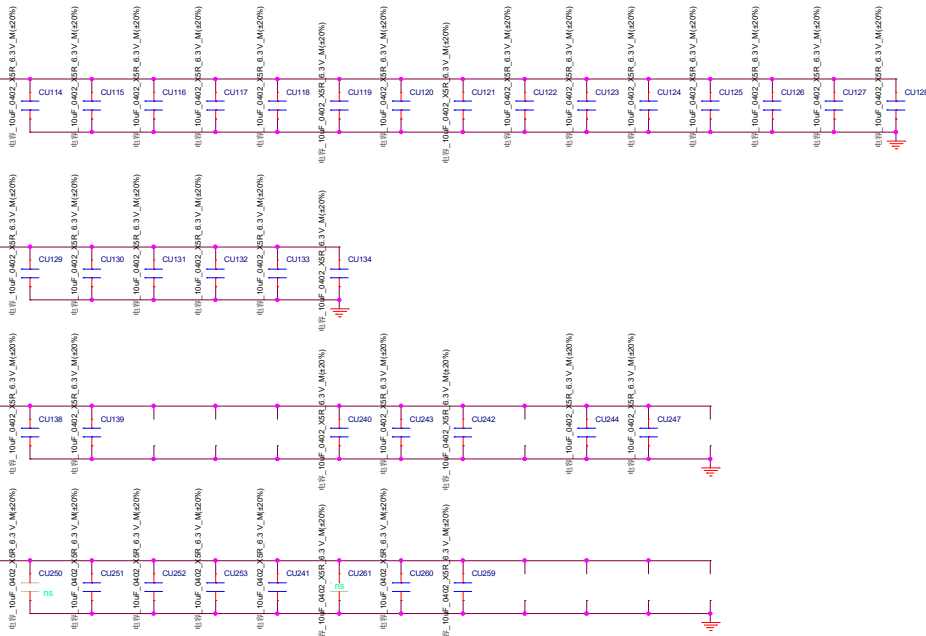


+VCCIN_AUX

PLACE THESE CAPS UNDERNEATH BOA AREA



PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

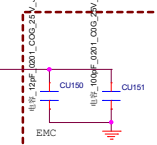
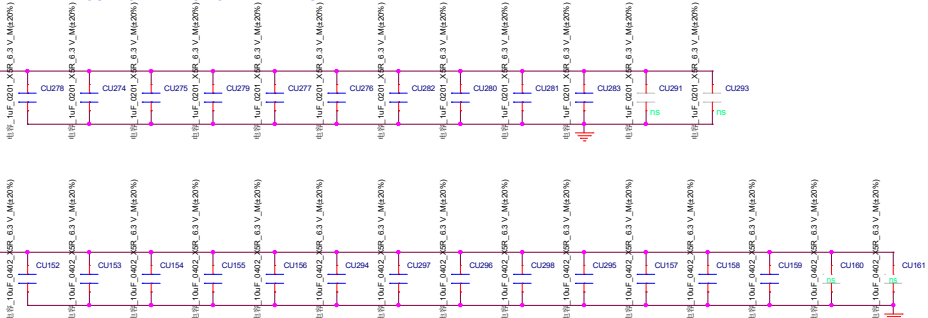


+VCCIN_AUX

	PDG	NB2608	
1uF		12(B)	
10uF	15(T)+10(B)	21	
22uF	12	24	
47uF	3+3(NC)	0	
220uF	1	0	

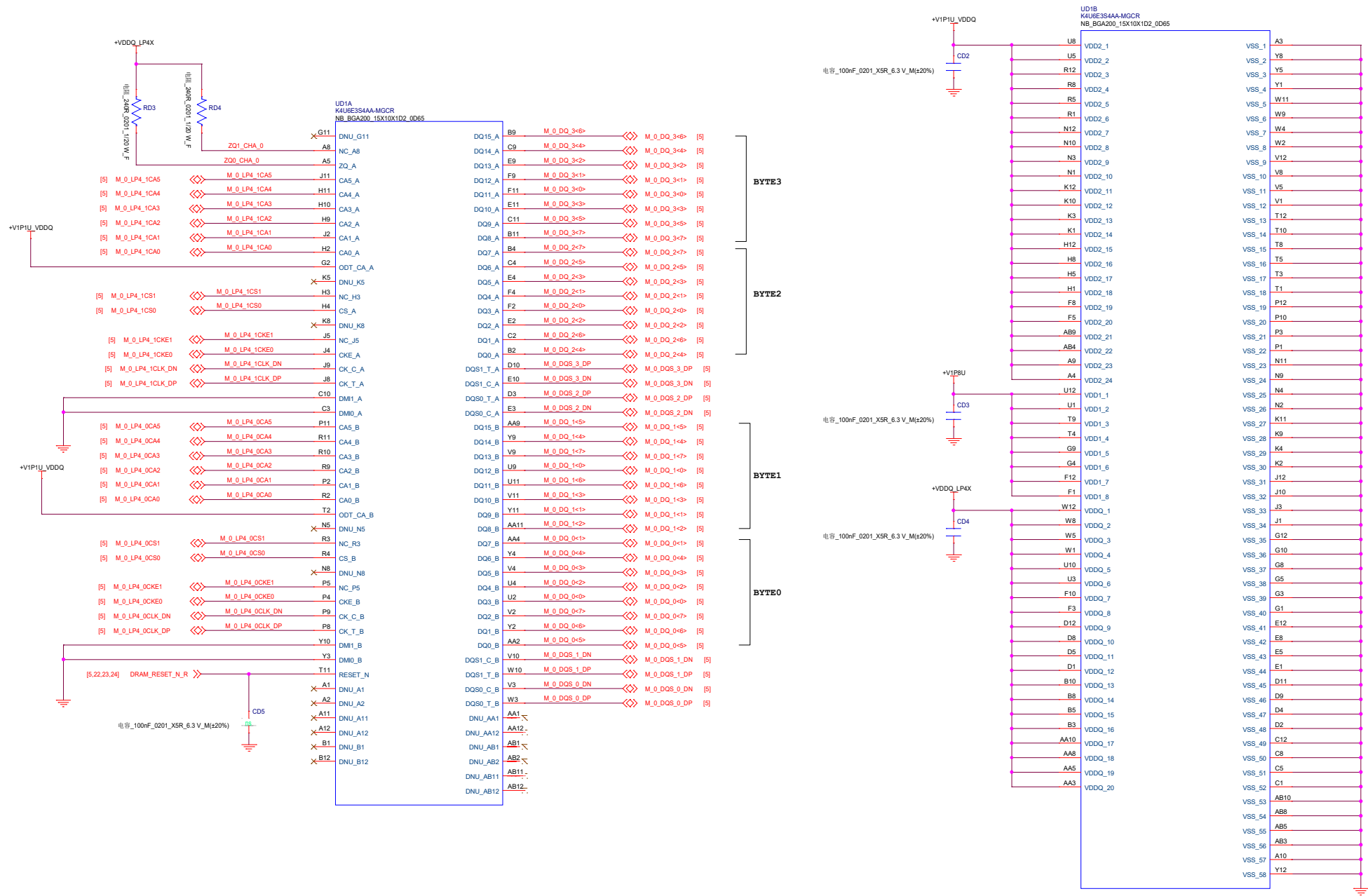
+VDDQ_CPU

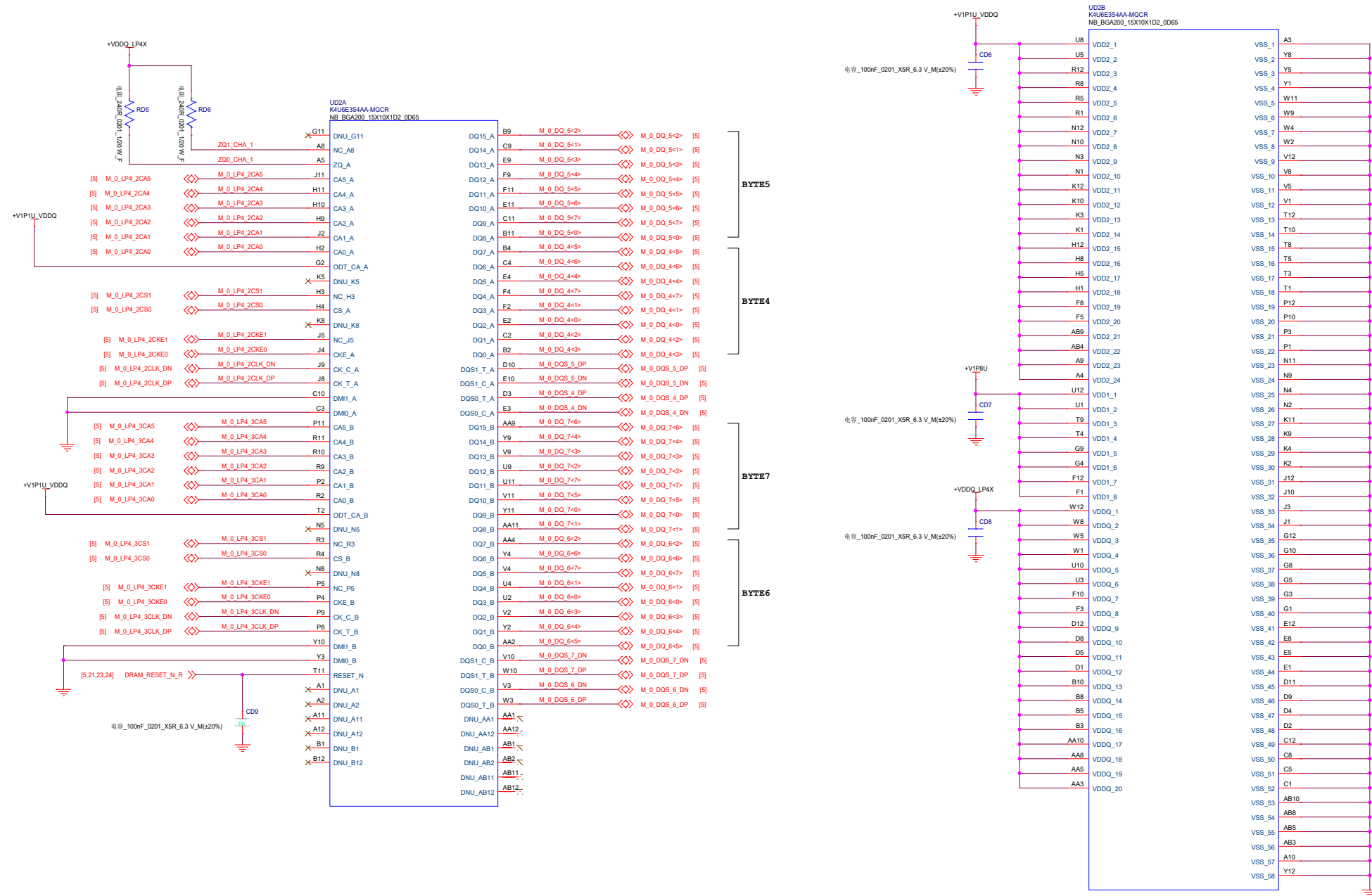
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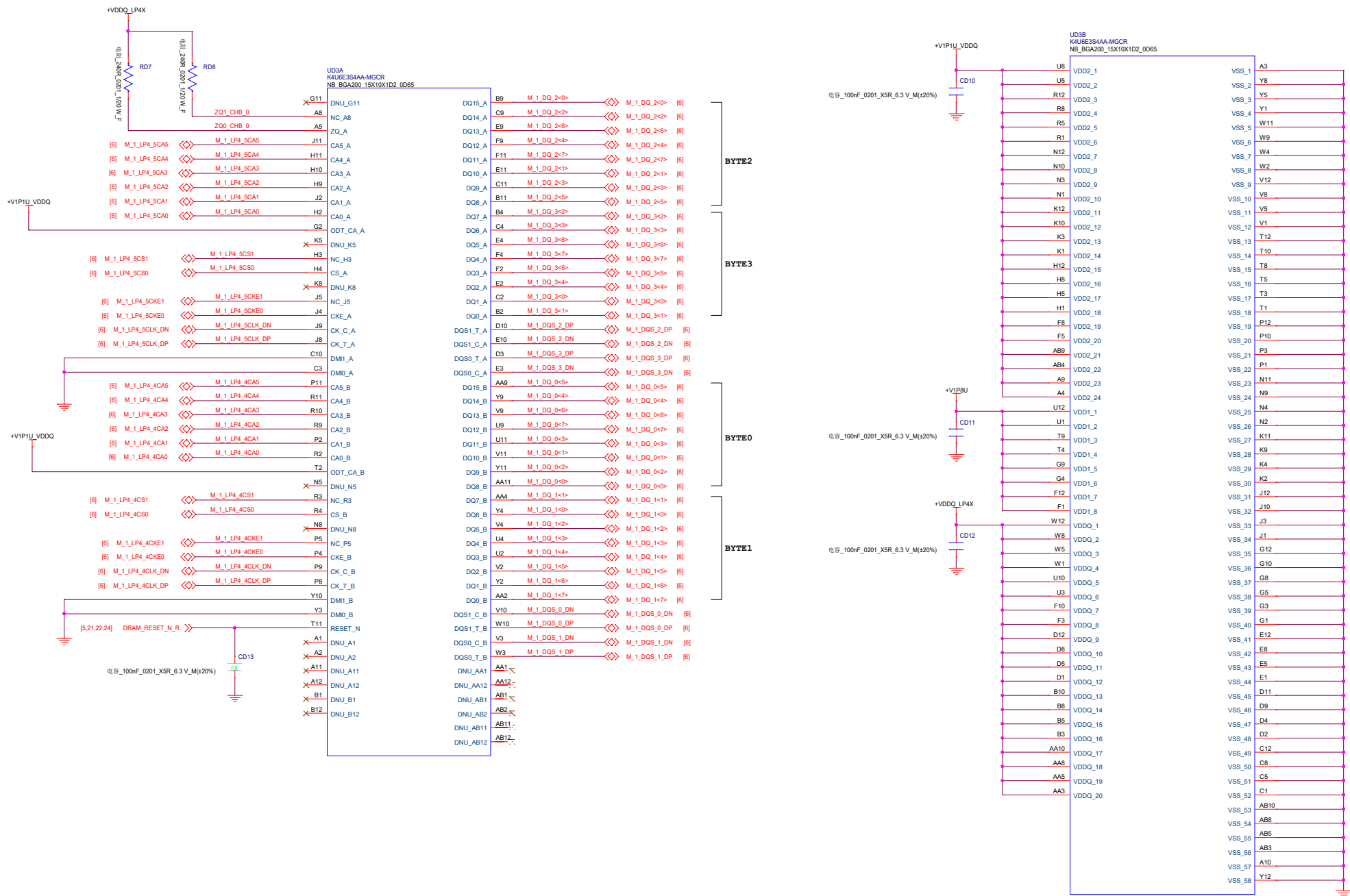


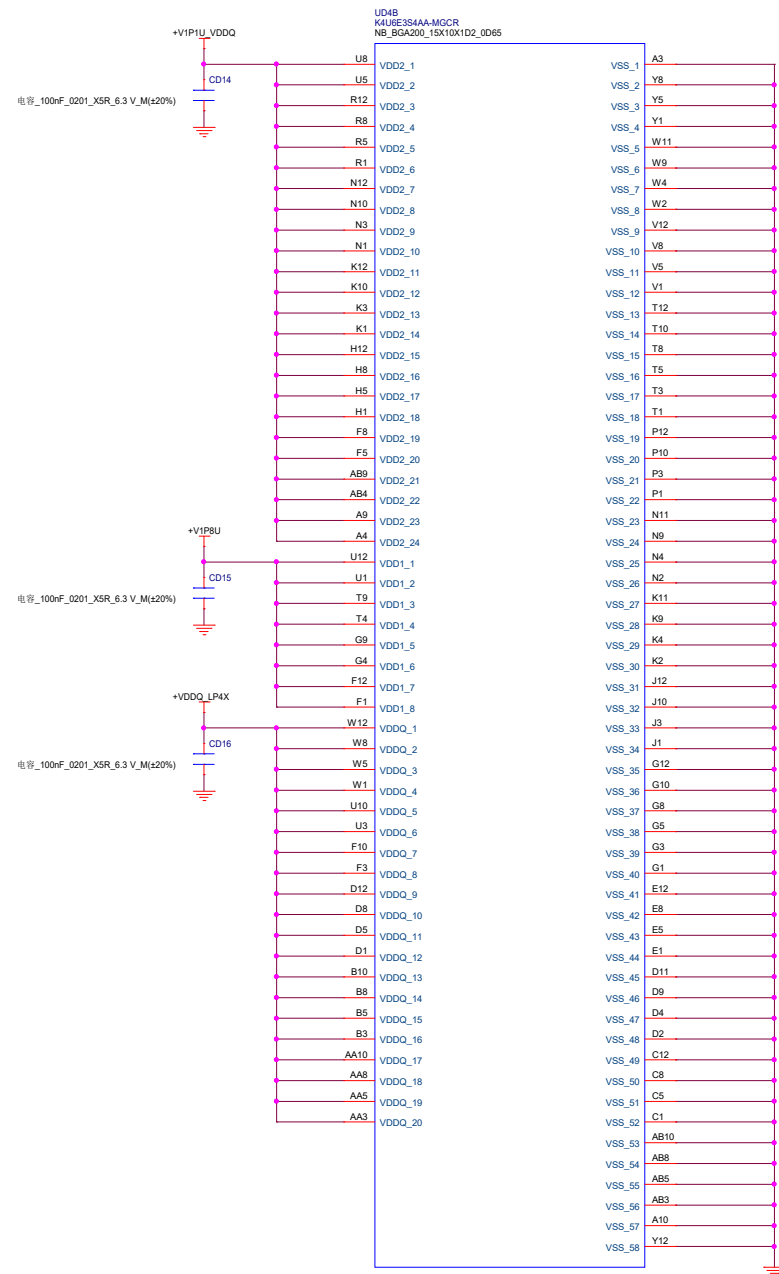
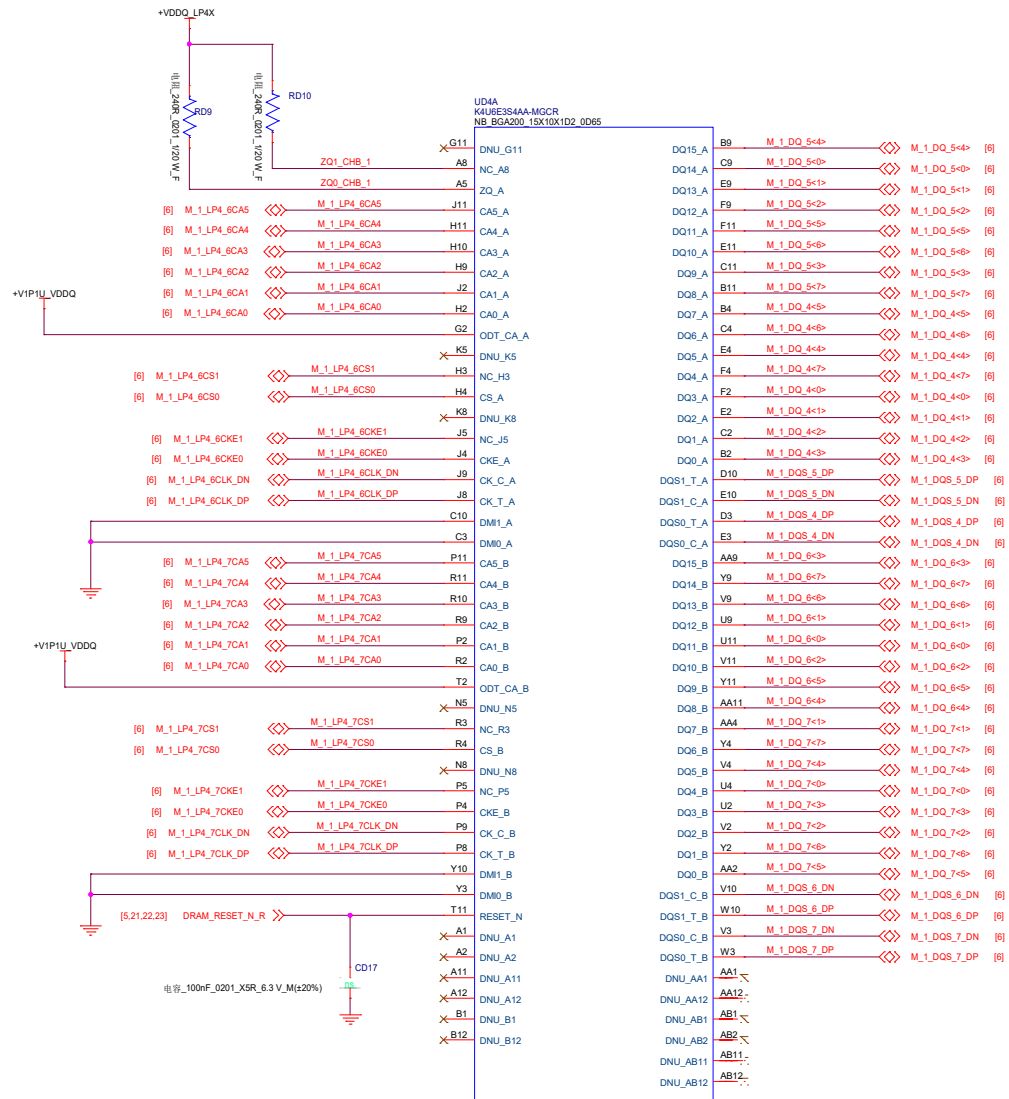
+VDDQ_CPU/VDD2

	PDG	NB2608
1uF	8	8
10uF	13	13
22uF		
47uF	2	Close to VR

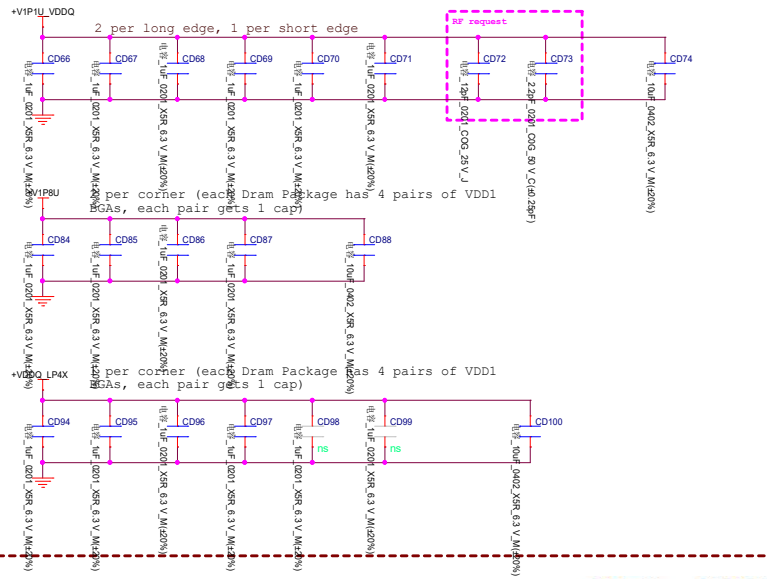
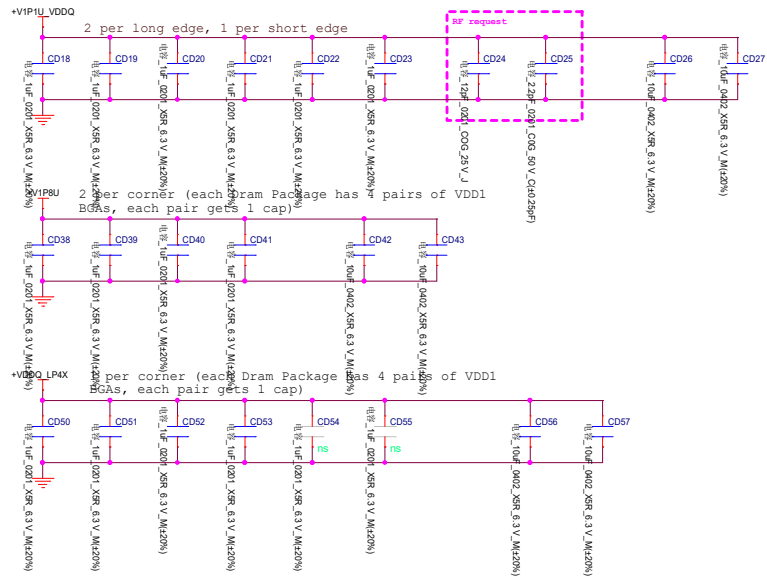








DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL A



DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL B

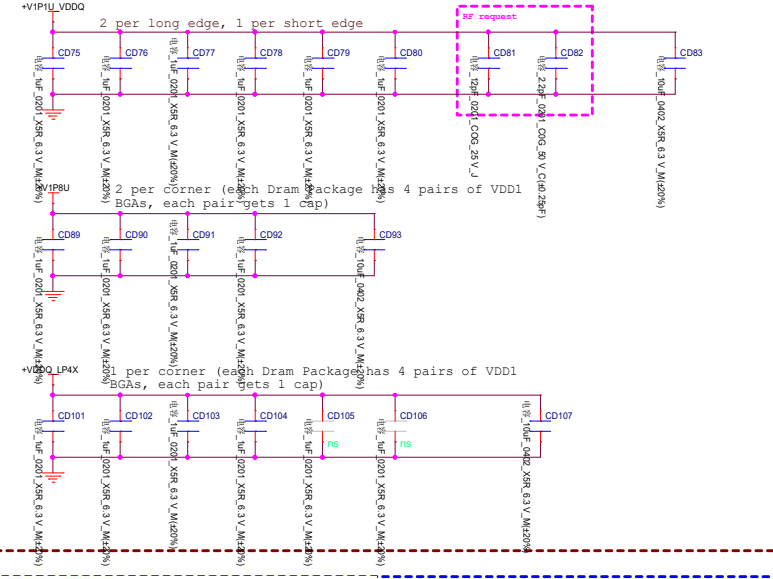
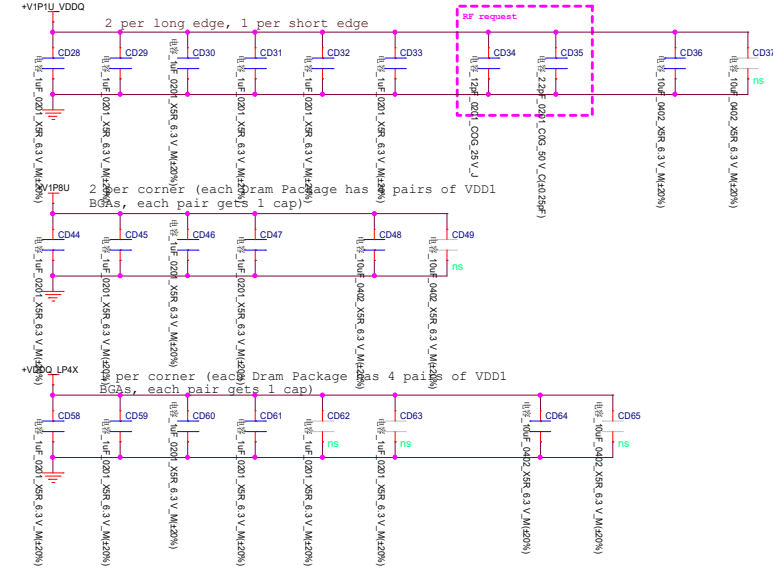
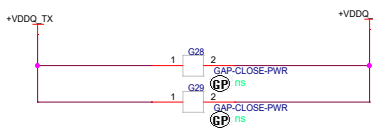



Table 48. LPDDR4x Memory Down Power Plane Decoupling

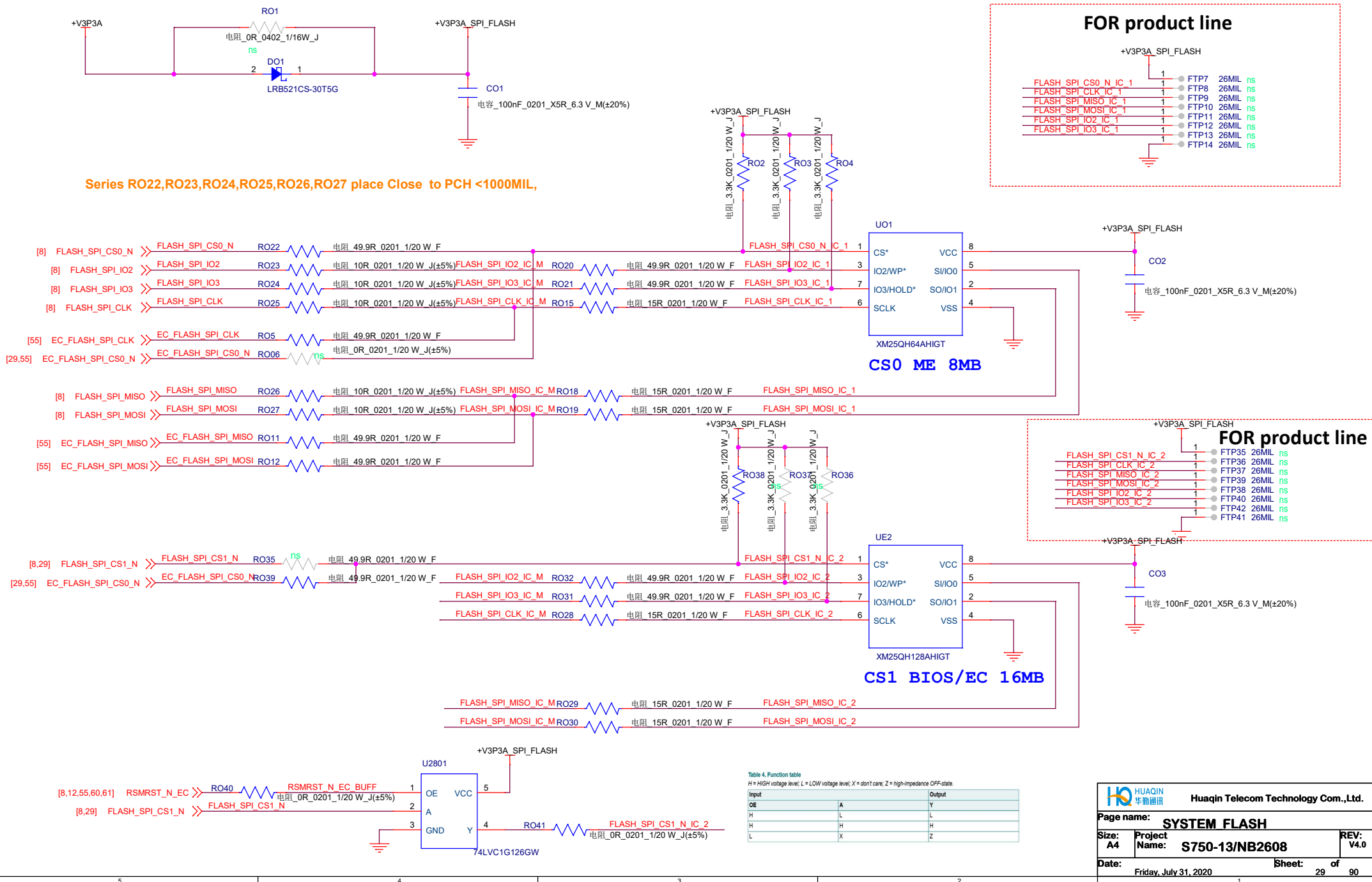
Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4x x32 Decoupling Config-1	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge evenly distribute among all Drams	24x 1 μ F (0402) 5x 10 μ F (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute among all Drams	16x 1 μ F (0402) 5x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μ F (0402)



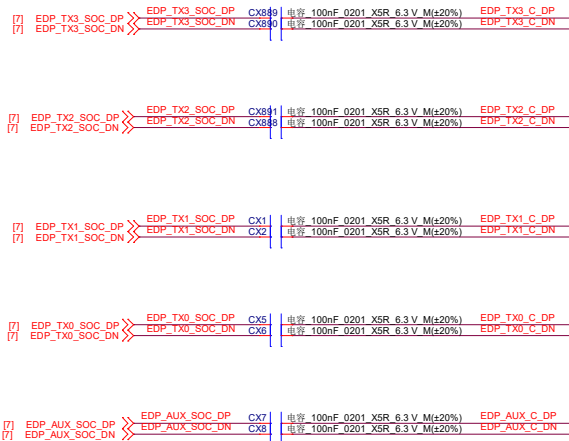
5	4	3	2	1
D				
C				
B				
A				
5	4	3	2	1

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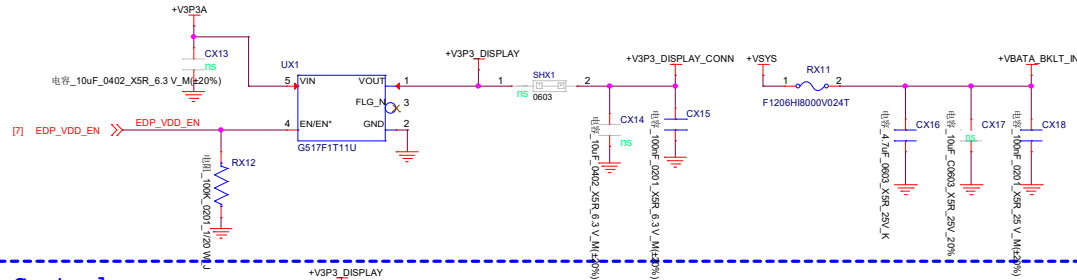
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D									
C									
B									
A									
5		4		3		2		1	



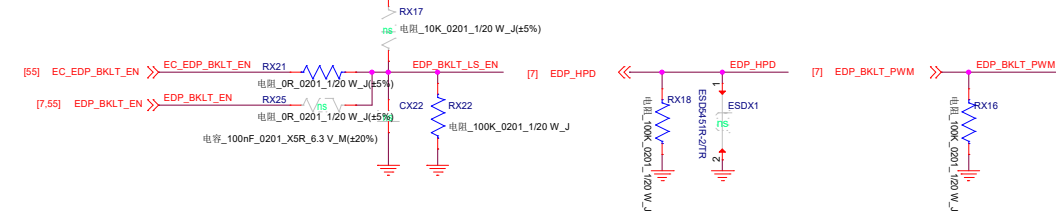
eDP Signal



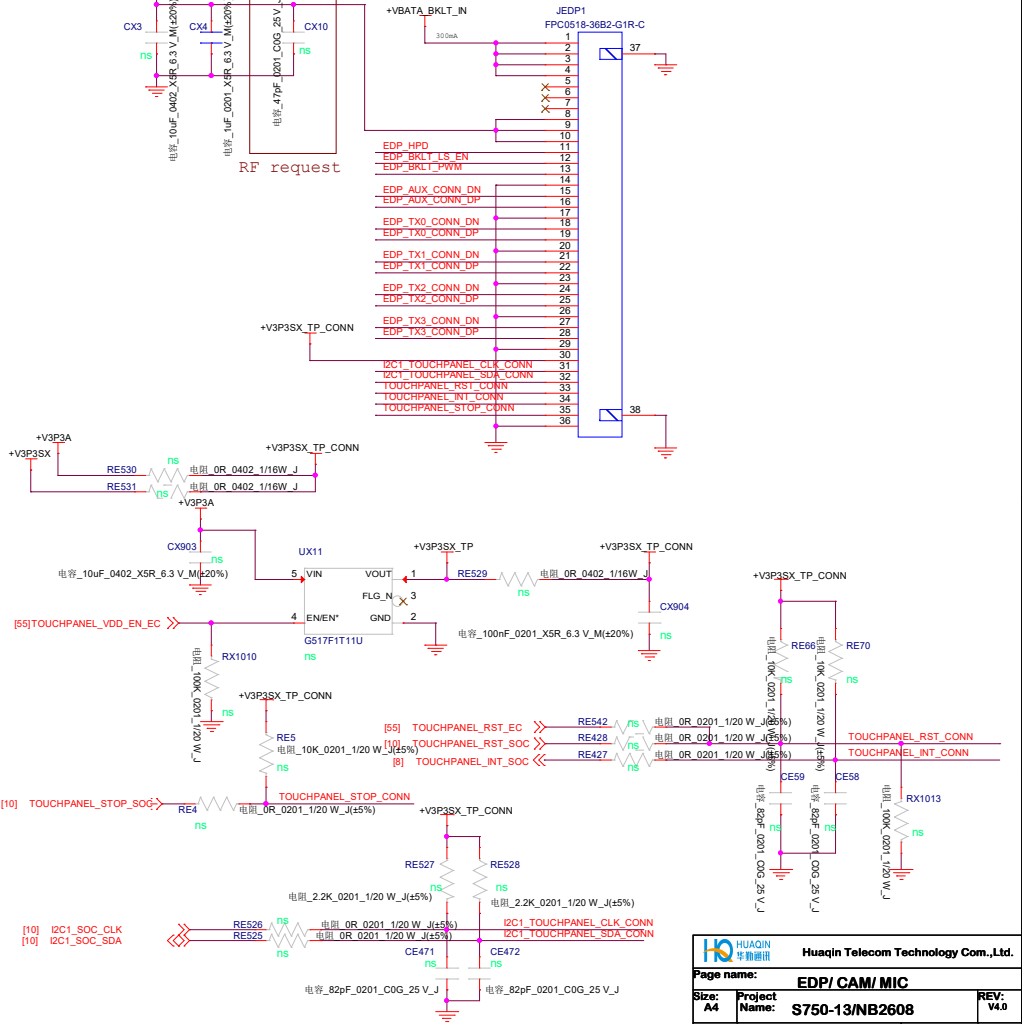
eDP VCC & BL Power

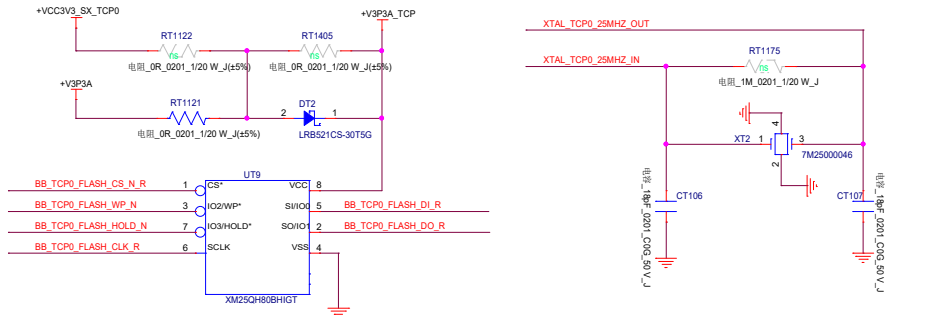
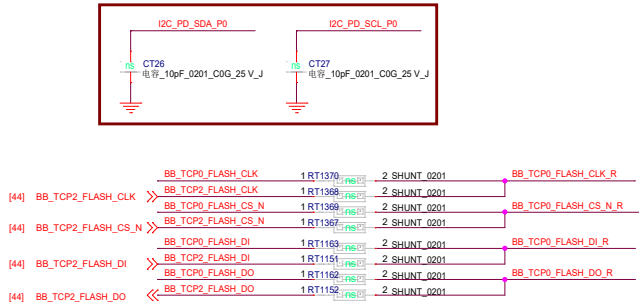
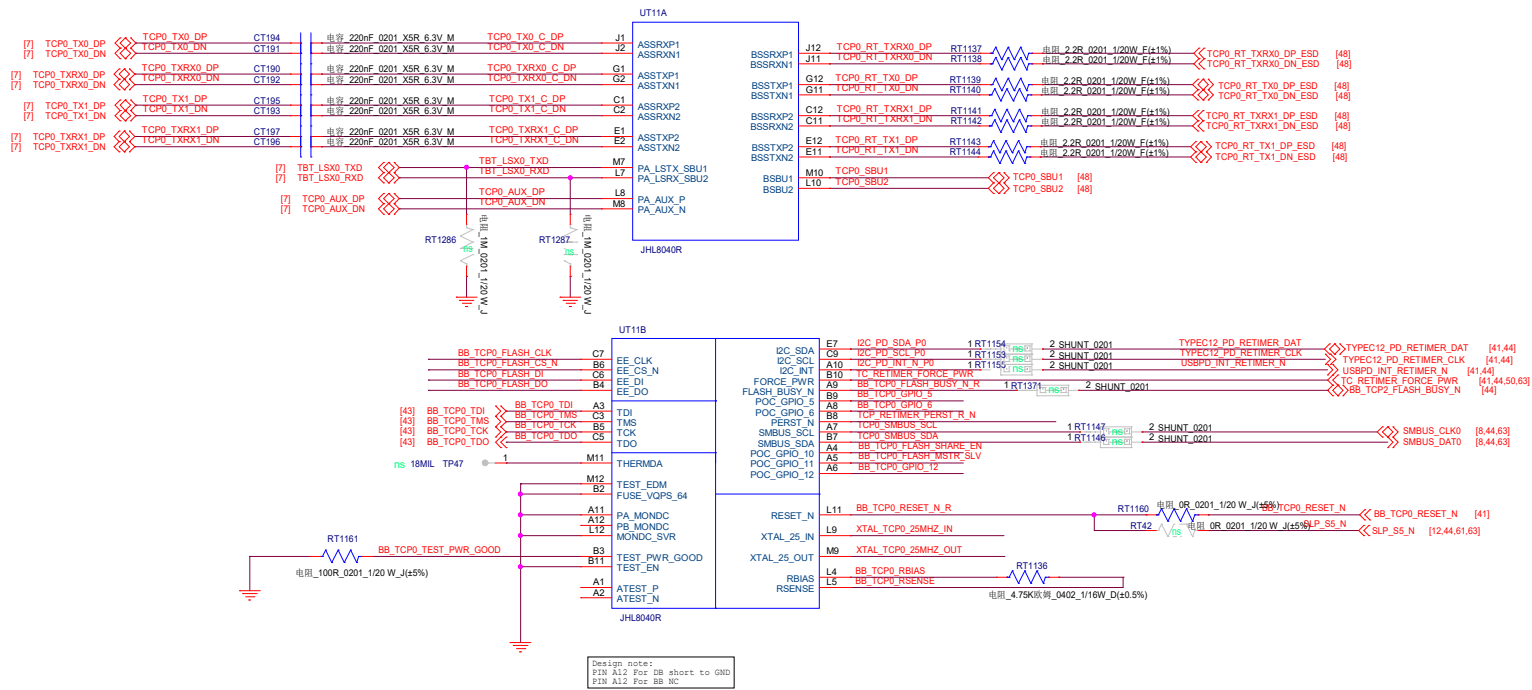


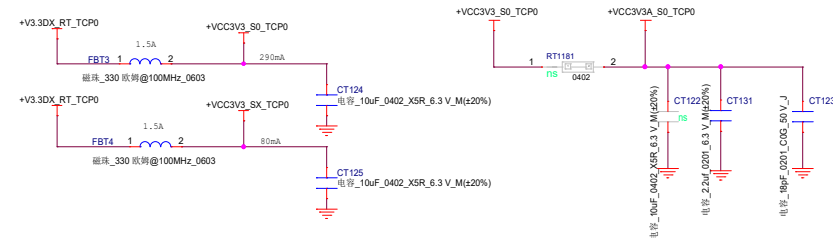
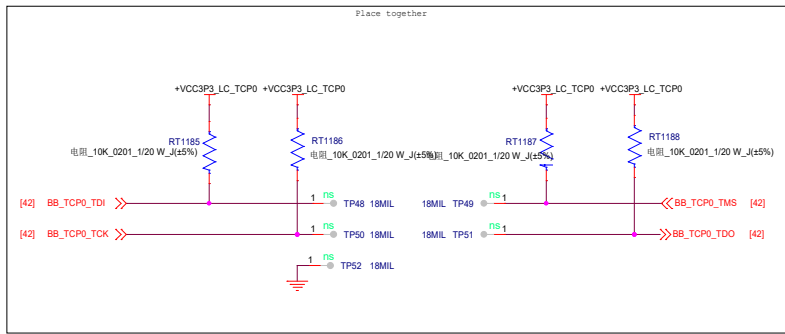
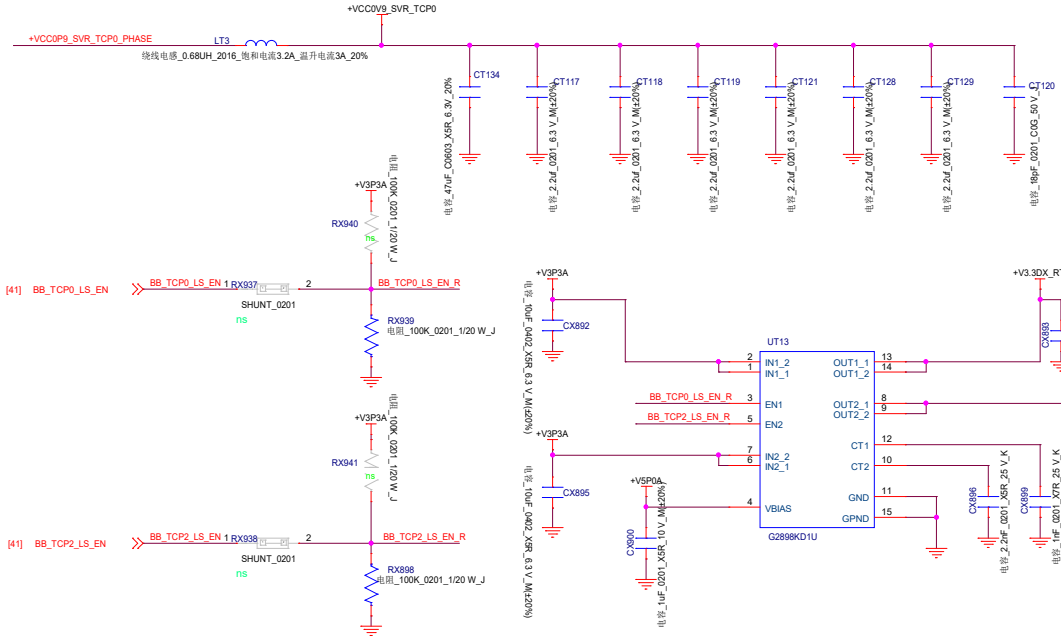
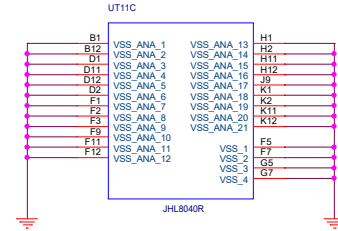
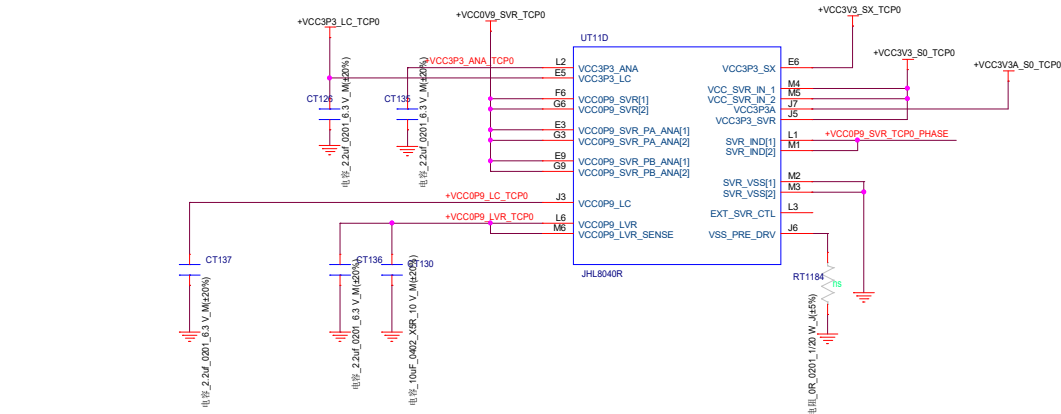
eDP Control

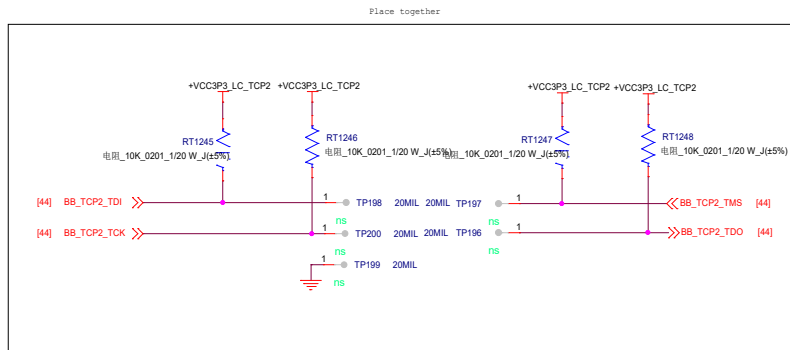
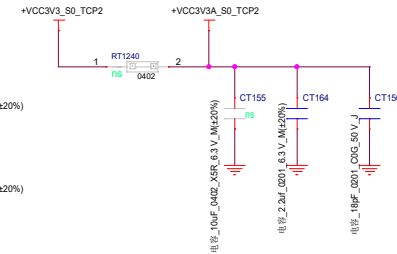
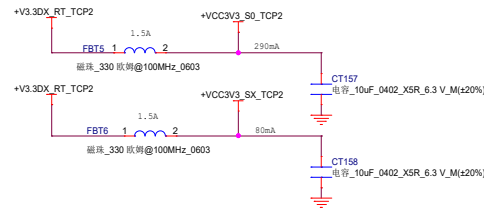
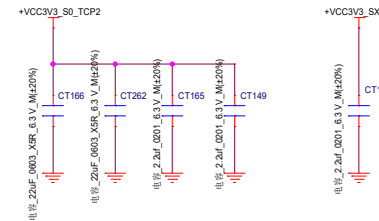
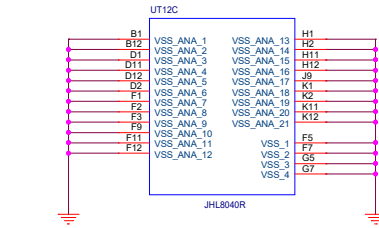
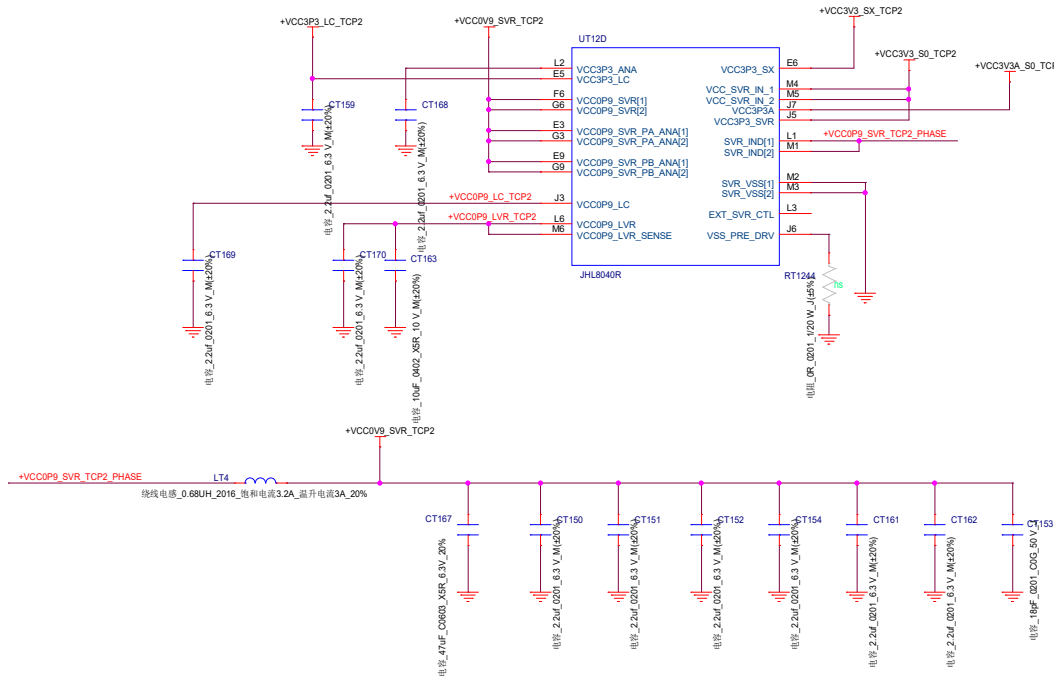


eDP CONN









TYPE-C PD INPUT

The schematic diagram illustrates the Type-C PD Input circuit. It features two MOSFETs, QT15 (PE5E8BA) and QT14 (PE5E4BA), connected in a push-pull configuration. The gates of these MOSFETs are driven by PD1_PA_GATE_VBUS and PD1_PA_GATE_VSYS signals through a network of resistors (RT1415, RT1416) and a shunt (SHUNT_0201). A capacitor CT275 is connected to the gates. The drains of the MOSFETs are connected to +VBUS_TYPEC_PP_HV and +VBUS_TYPEC1. A 100nF capacitor is connected to the gates. The circuit is labeled with various components and their values.

Component values and labels:

- RT1415: 1 RT1415
- RT1416: 1 RT1416
- SHUNT_0201: 2 SHUNT_0201
- CT275: CT275
- QT15: PE5E8BA
- QT14: PE5E4BA
- +VBUS_TYPEC1
- +VBUS_TYPEC_PP_HV
- PD1_PA_GATE_VBUS
- PD1_PA_GATE_VSYS
- PD1_PA_GATE_VBUS_G
- PD1_PA_GATE_VSYS_G

Page name: TYPE C Power 1

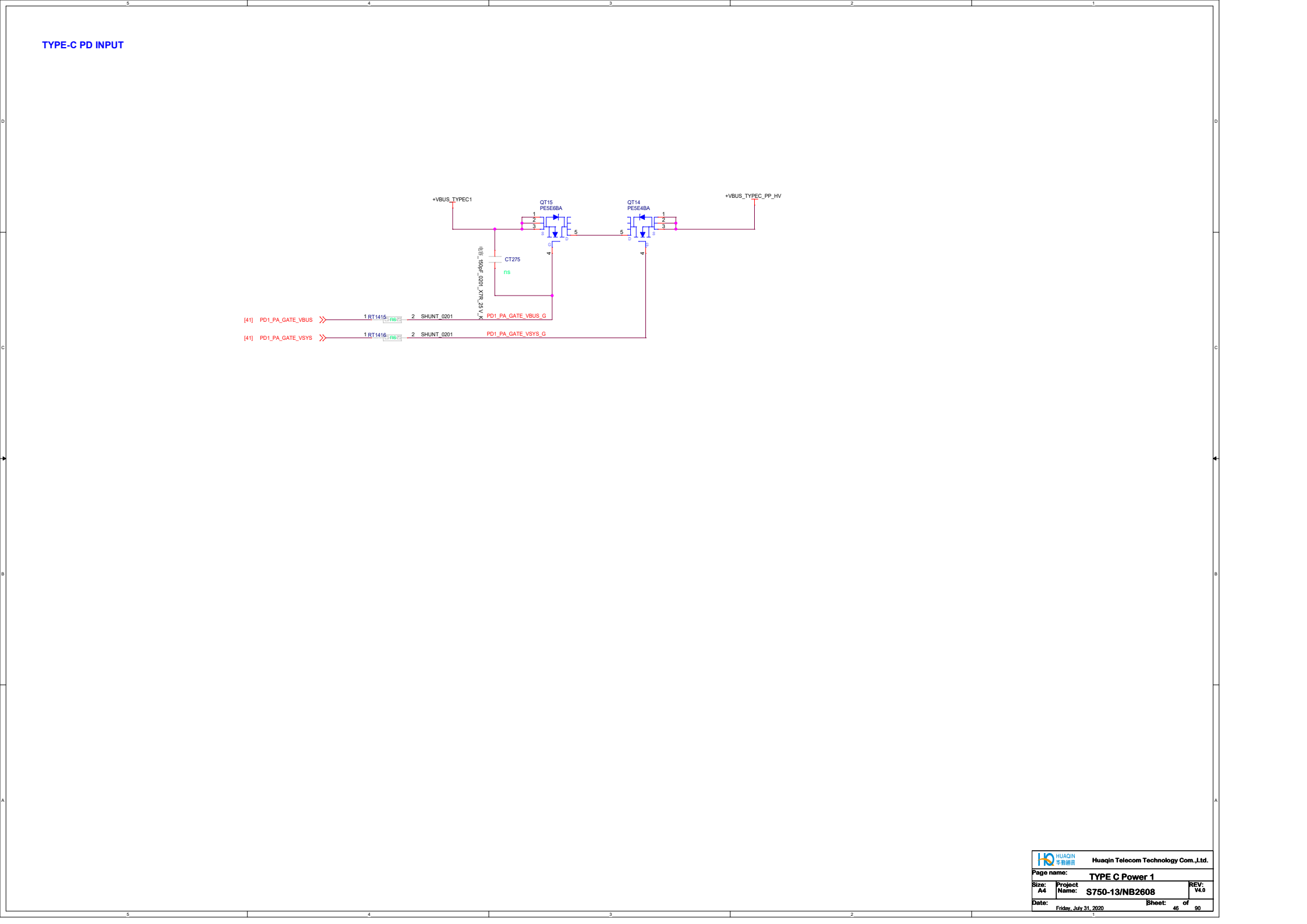
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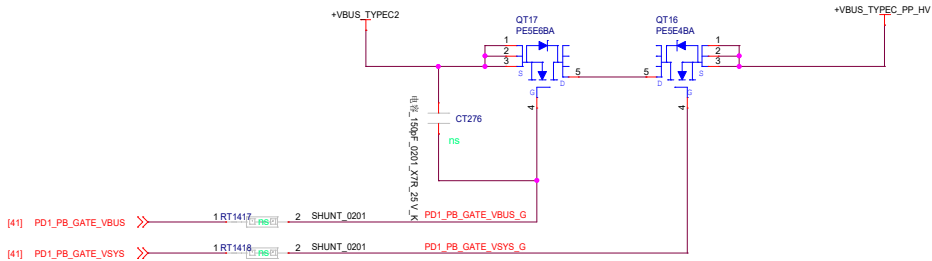
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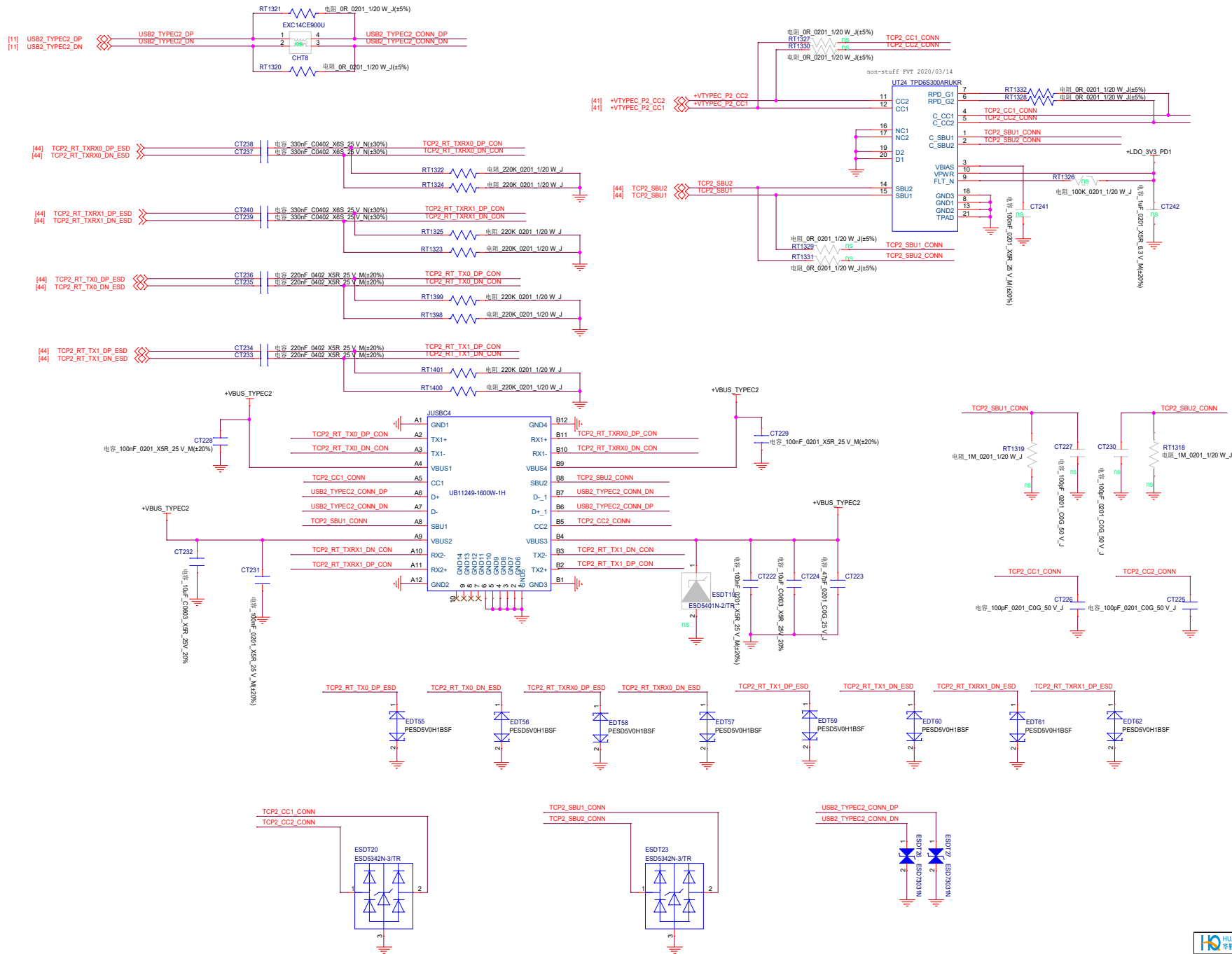
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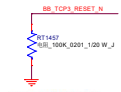
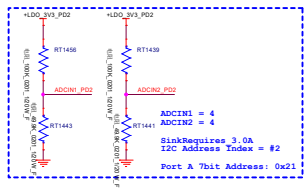
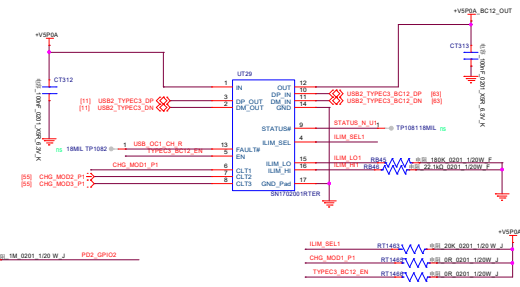
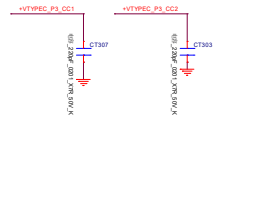
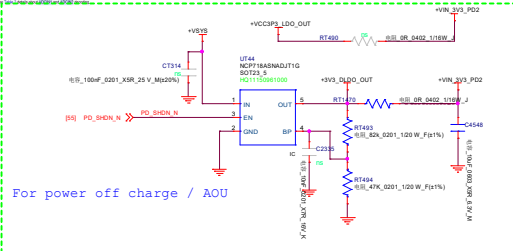
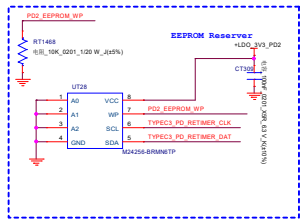
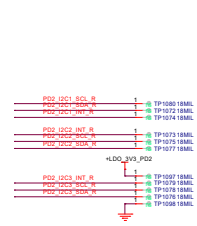
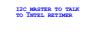


TYPE-C PD INPUT

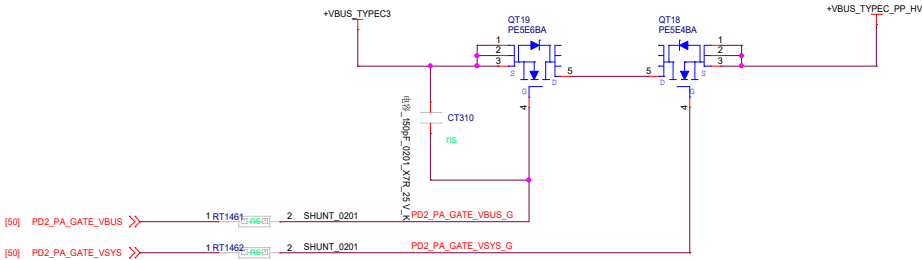




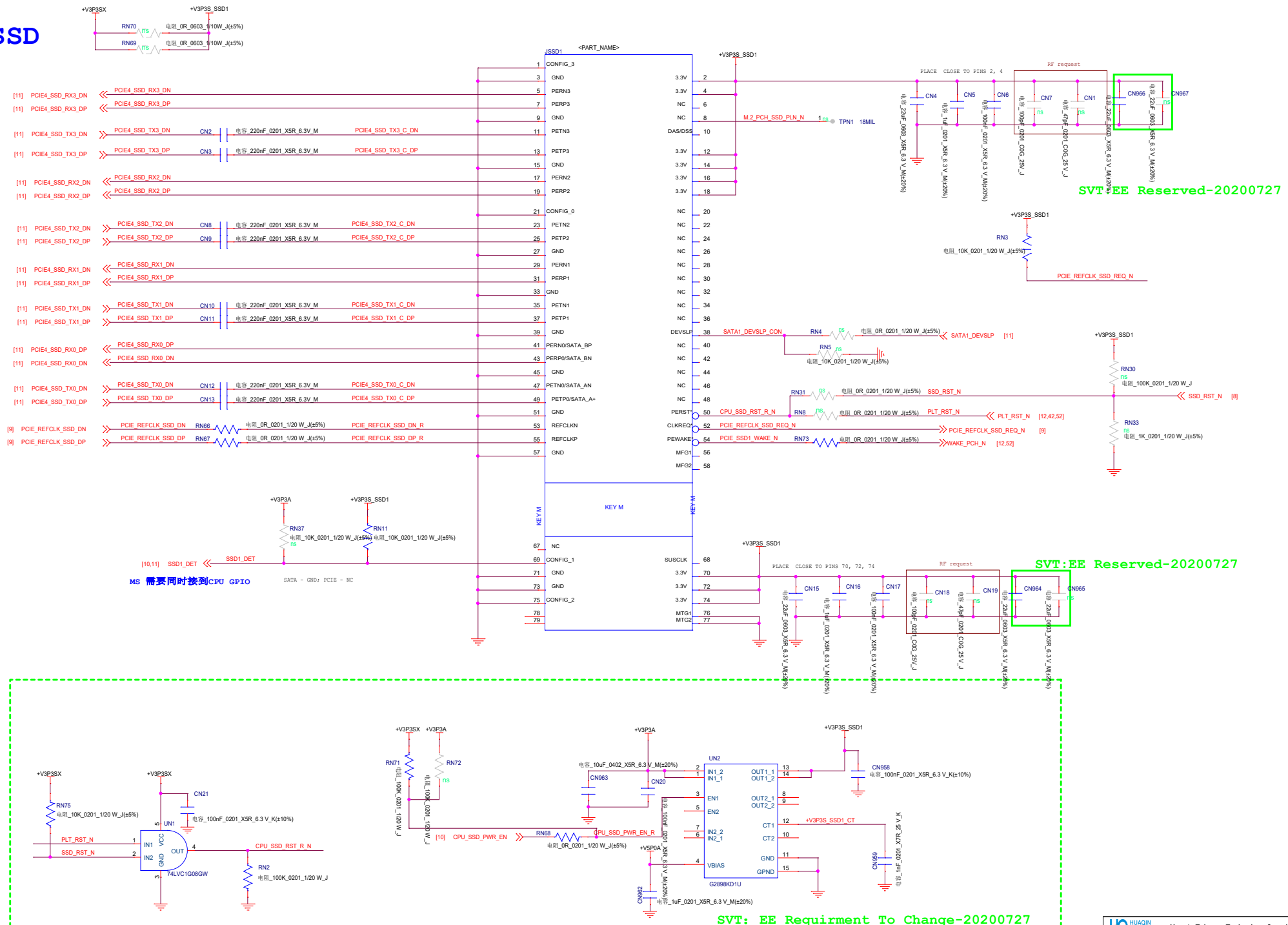
Type-C 3 PD

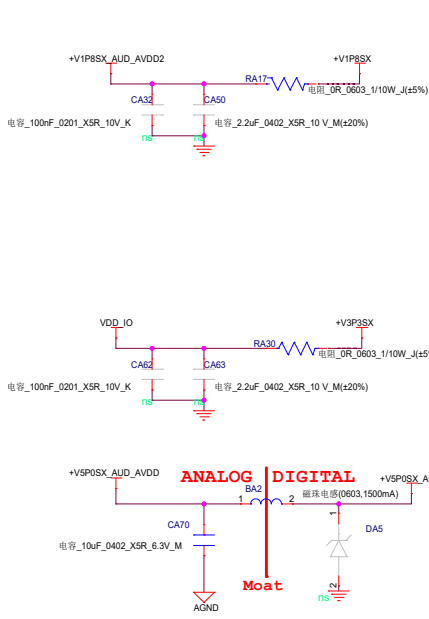
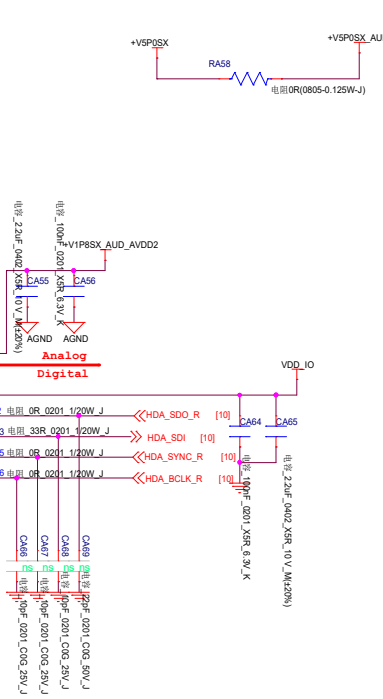
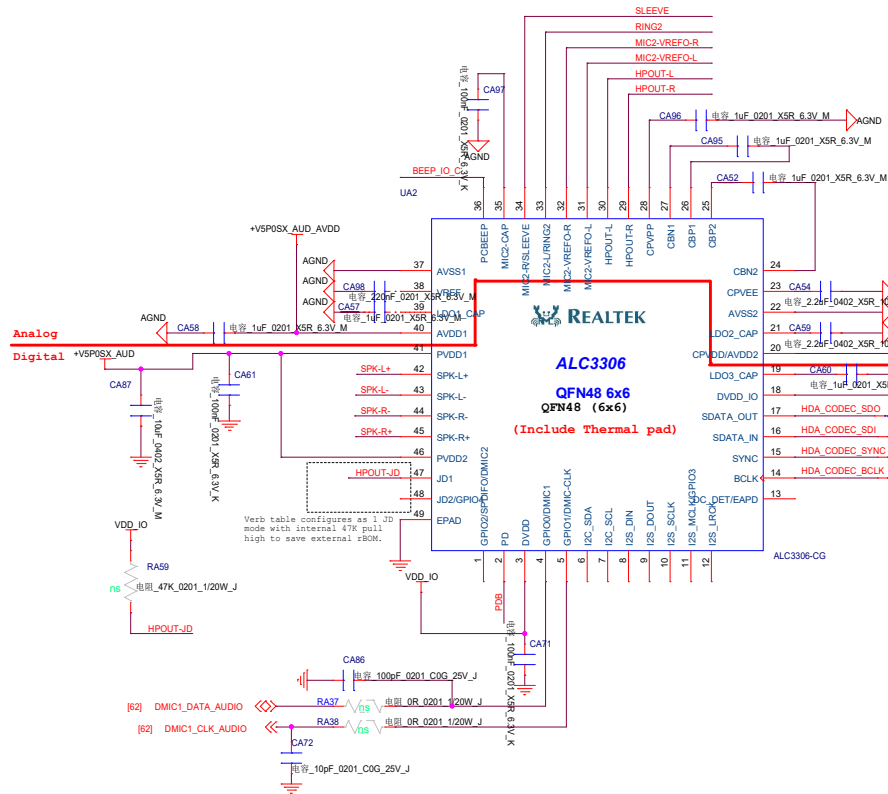
[illegible]

Type-C 3 PWR INPUT

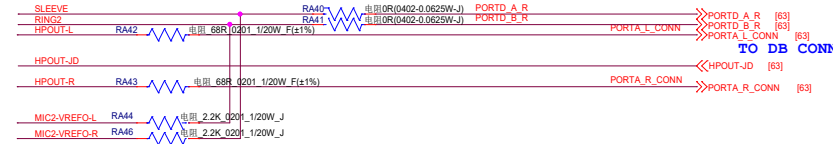


SSD

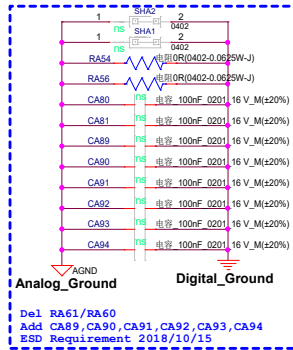
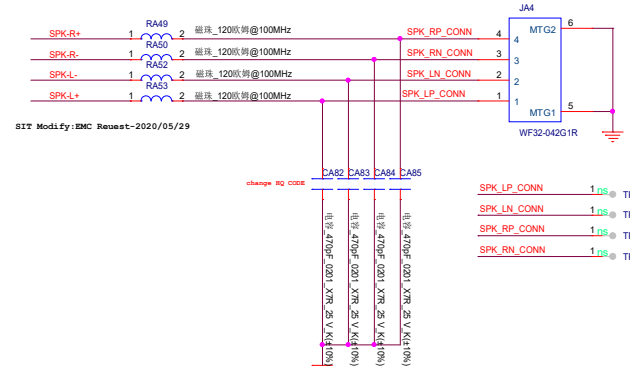


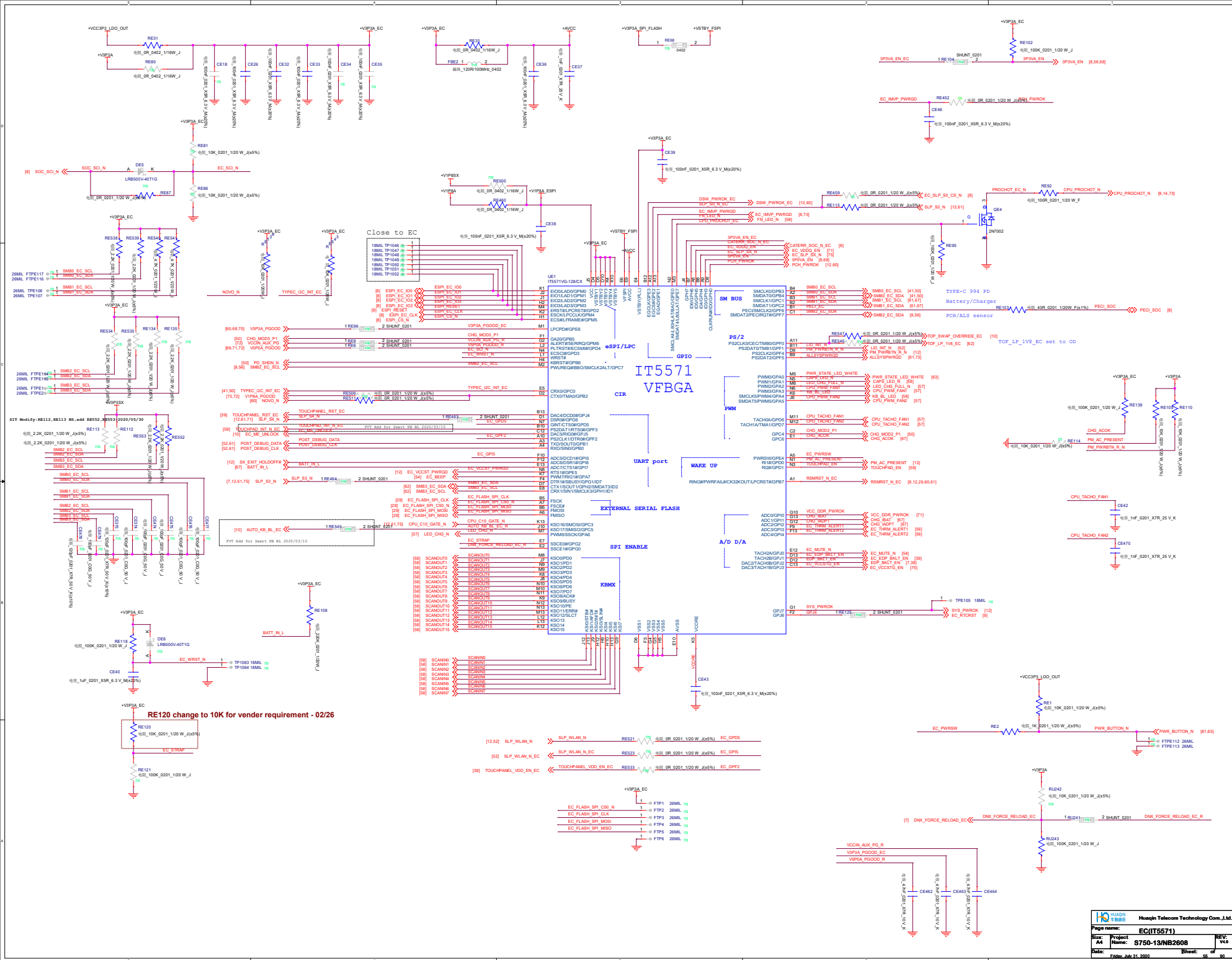


Global Headset Jack with 2Vrms and 120dB SNR.
Headphone / Line Out / CTIA & OMTp



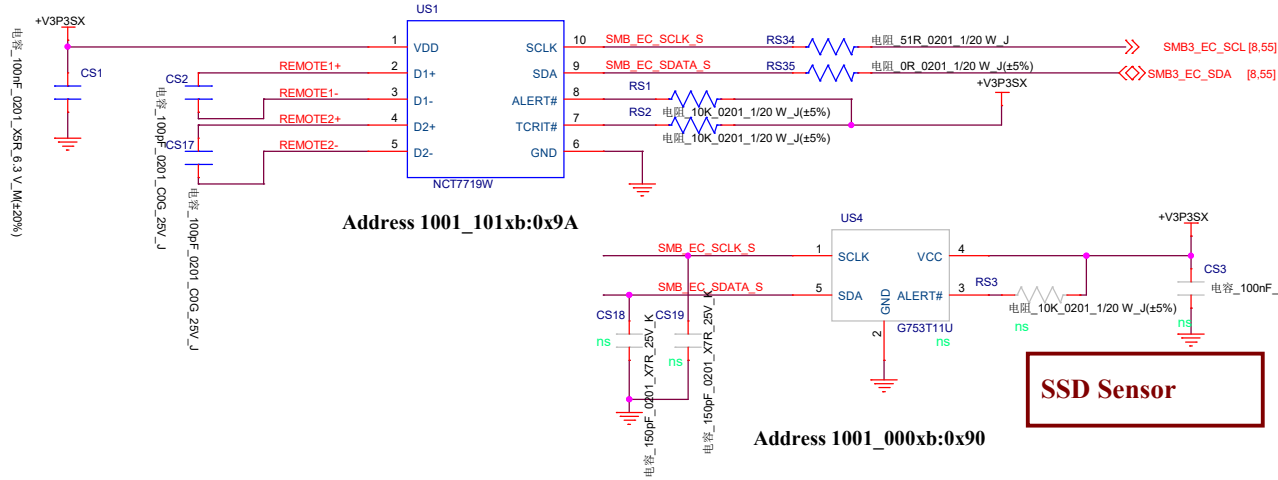
Internal Speaker connector
Placement near Audio Codec
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils





REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces

CPU Sensor

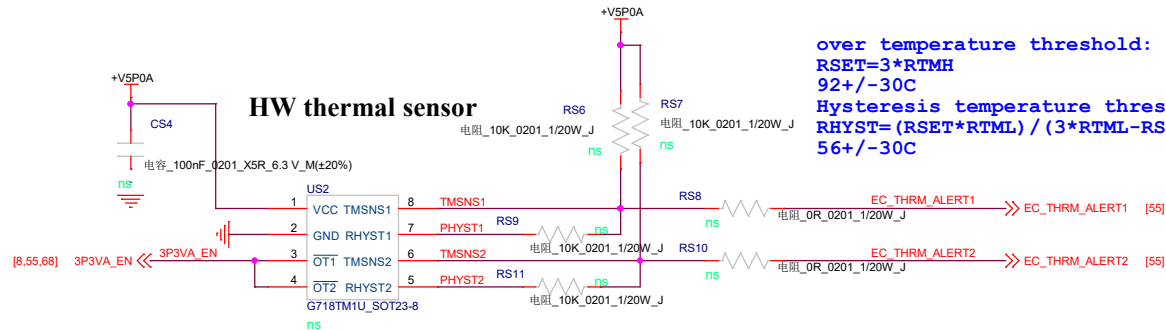


Ambient Sensor

Charger Sensor

SSD Sensor

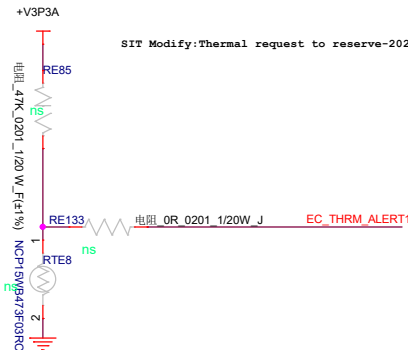
HW thermal sensor



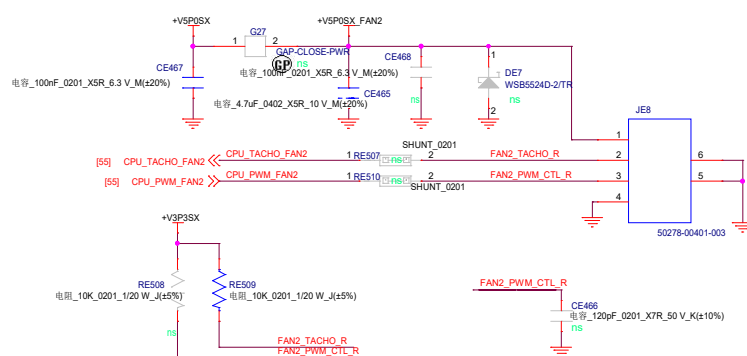
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

NOTE:
HW thermal sensor??

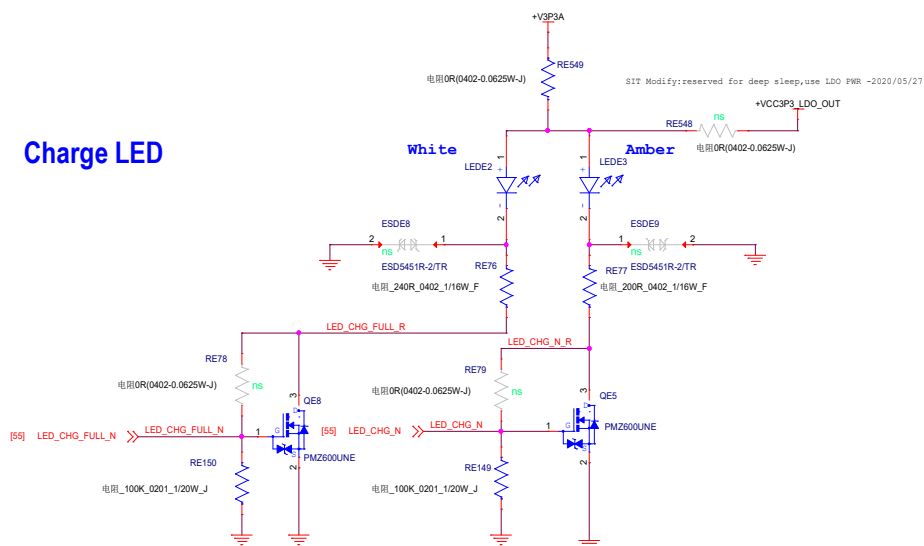
SIT Modify:Thermal request to reserve-2020/05/29



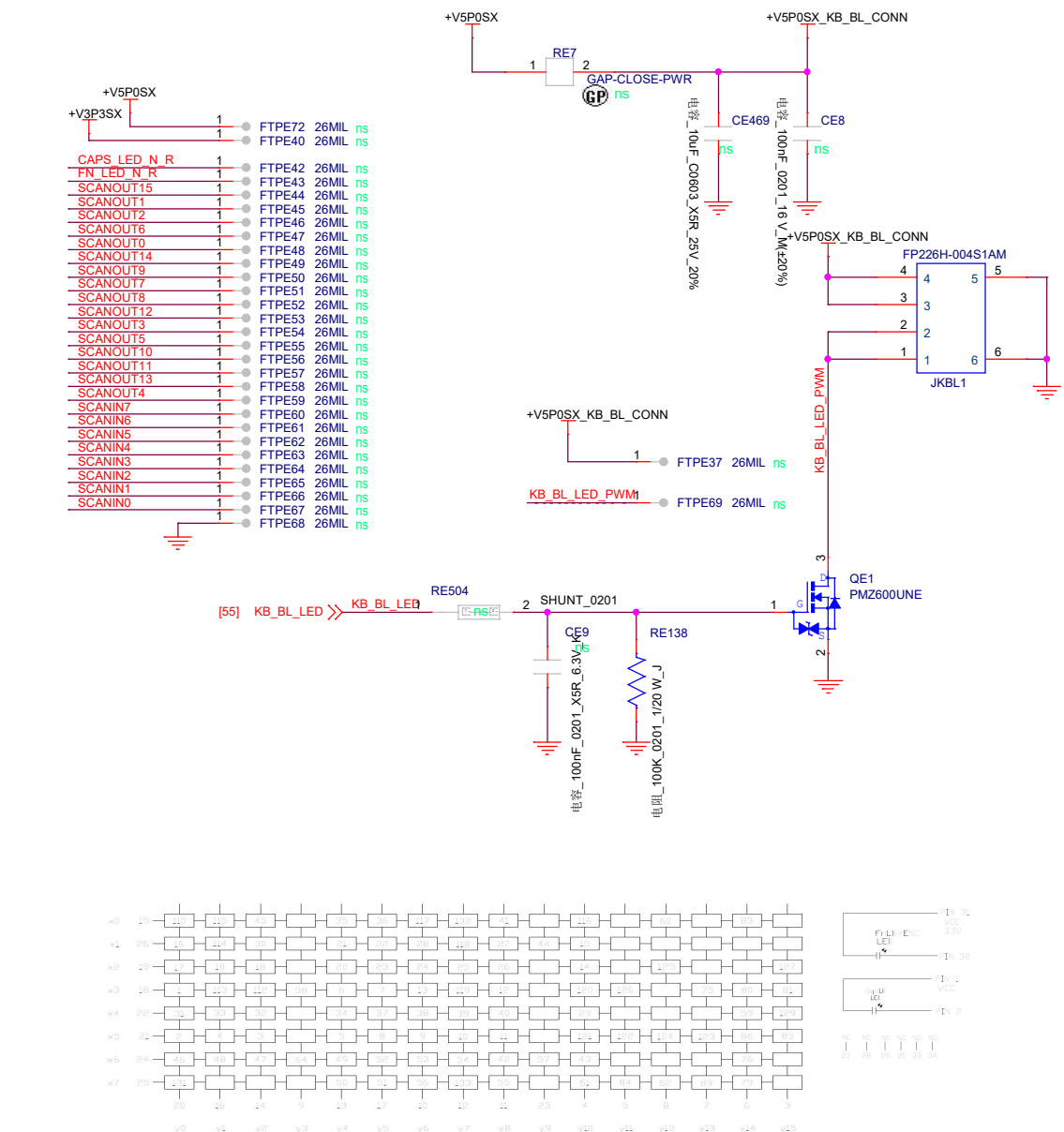
FOR product line



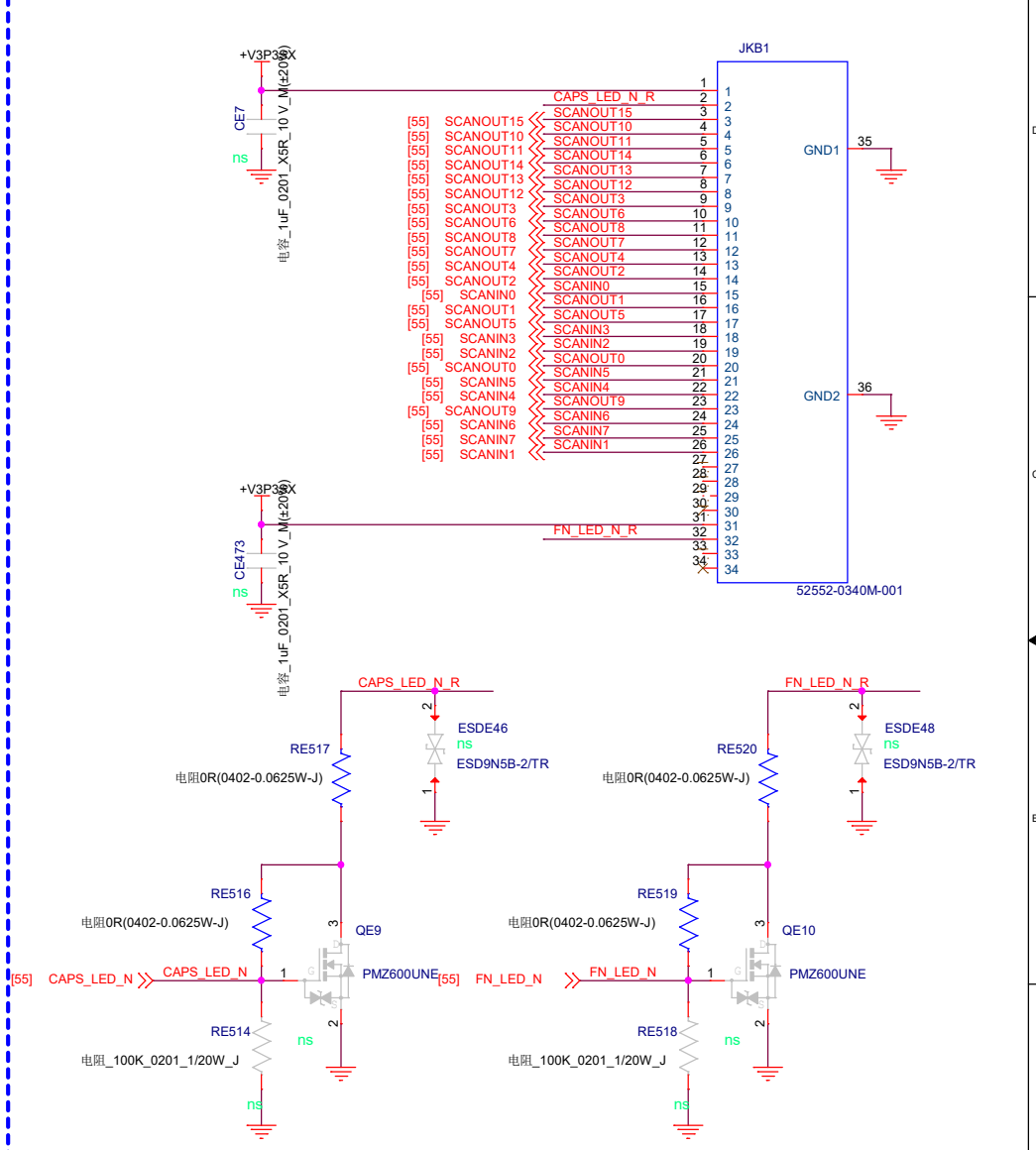
Charge LED



KB Backlight

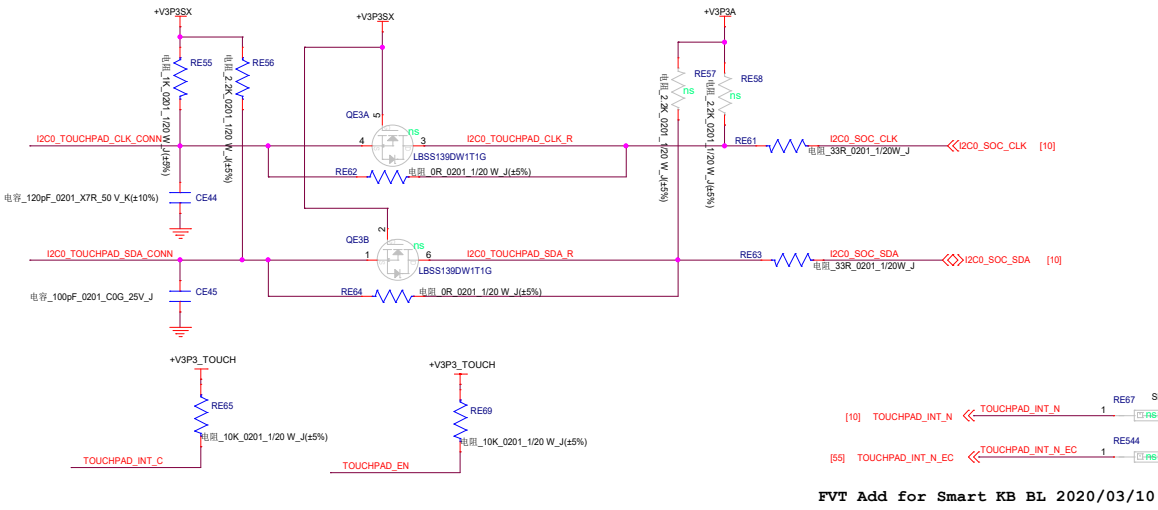


KB CONN

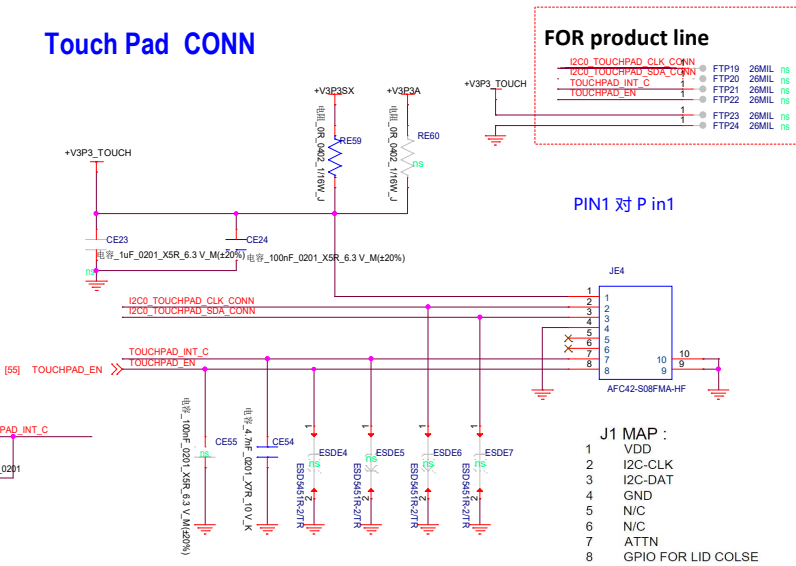


Connected directly to a supply, usually 3 - 3.3V, and no series resistor is required.

Touch Pad



Touch Pad CONN

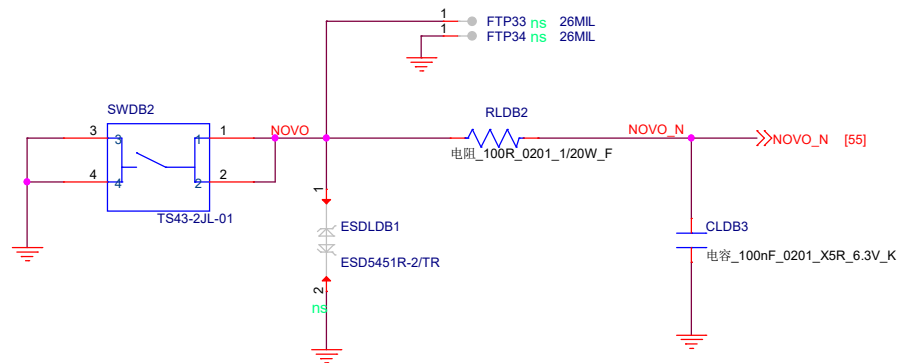



PIN1 对 P in1

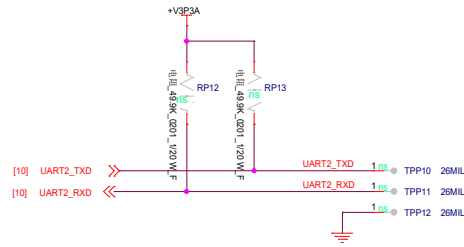
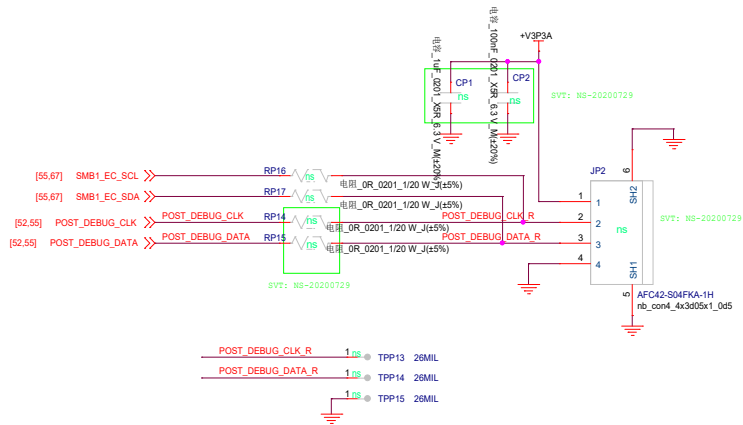
- J1 MAP :
- 1 VDD
 - 2 I2C-CLK
 - 3 I2C-DAT
 - 4 GND
 - 5 N/C
 - 6 N/C
 - 7 ATTN
 - 8 GPIO FOR LID COLSE

Finger Print

Power BUTTON Move to DB



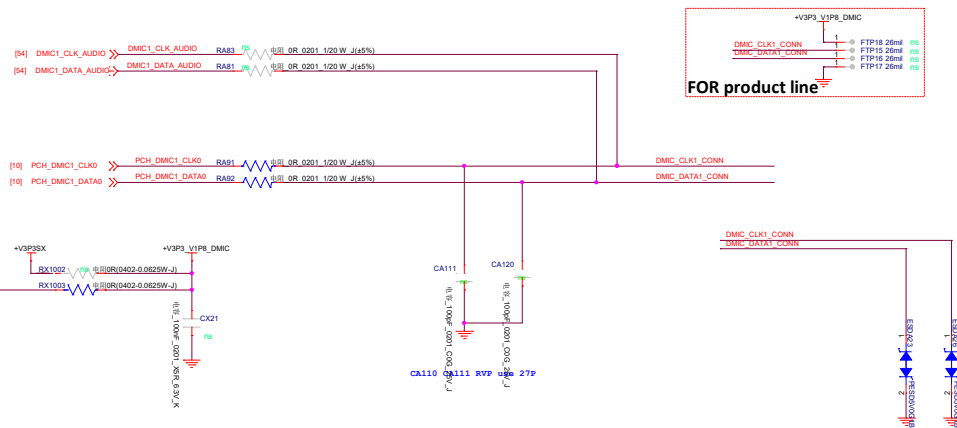
 HUAQIN 华勤通讯	Huaqin Telecom Technology Co., Ltd.	
Page name:		
Logic Circuit		
Size: A4	Project Name: S750-13/NB2608	REV: V4.0
Date: Friday, July 31, 2020	Sheet: 60	of 90



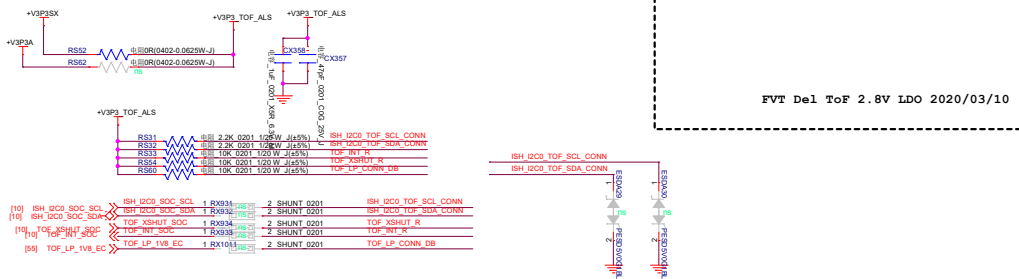
CMC

[8,12,29,55,60]	RSMRST_N_EC	>>	RSMRST_N_EC	1	TP1083	18MIL	ns
[12,70]	SLP_SUS_N	>>	SLP_SUS_N	1	TP1084	18MIL	ns
[12,42,44,63]	SLP_S5_N	>>	SLP_S5_N	1	TP1085	18MIL	ns
[12,55,71]	SLP_S4_N	>>	SLP_S4_N	1	TP1086	18MIL	ns
[7,12,55,75]	SLP_S3_N	>>	SLP_S3_N	1	TP1087	18MIL	ns
[12,55,75]	CPU_C10_GATE_N	>>	CPU_C10_GATE_N	1	TP1088	18MIL	ns
[12,55]	SLP_S0_N	>>	SLP_S0_N	1	TP1089	18MIL	ns
[55,73]	ALLSYSPWRGD	>>	ALLSYSPWRGD	1	TP1090	18MIL	ns
[55,63]	PWR_BUTTON_N	>>	PWR_BUTTON_N	1	TP1091	18MIL	ns
[12]	SLP_A_N	>>	SLP_A_N	1	TP1092	18MIL	ns
[12]	PLT_RST_SOC_N	>>	PLT_RST_SOC_N	1	TP1093	18MIL	ns

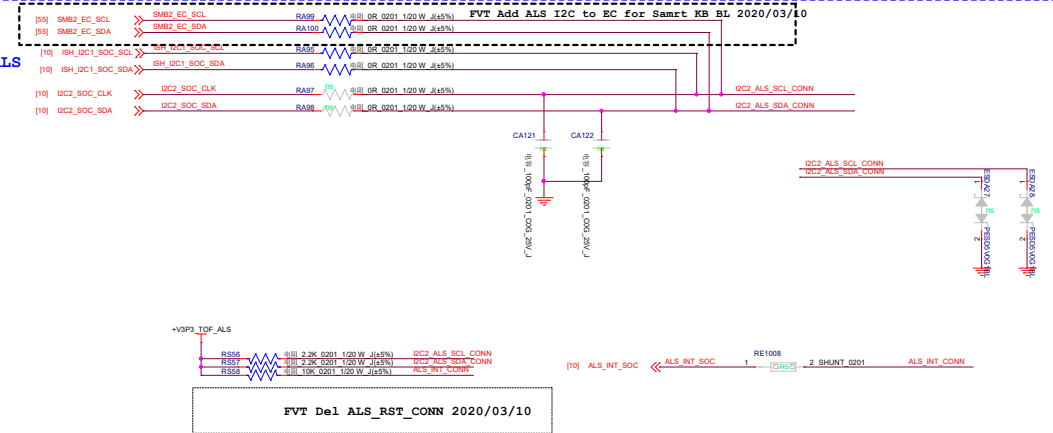
DMIC



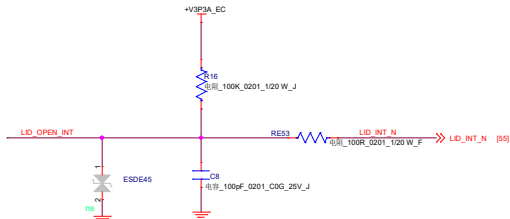
ToF Sensor



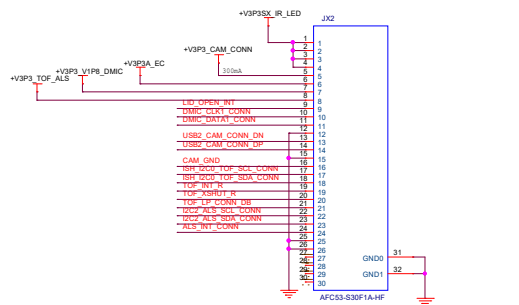
LS



Hall Sensor



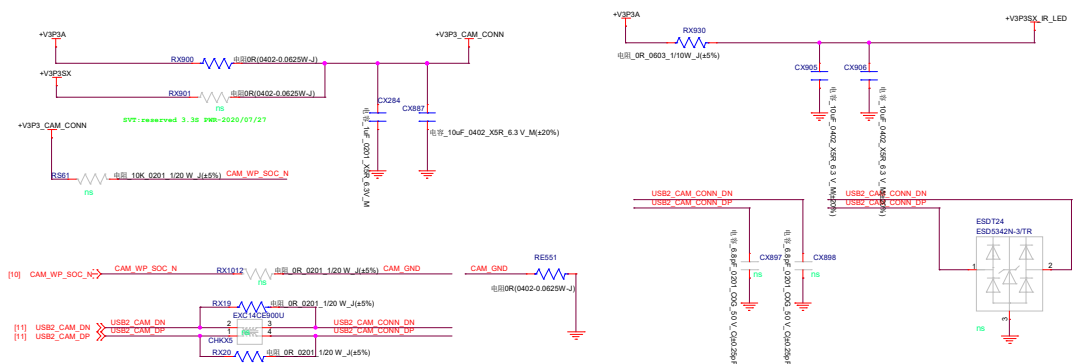
TOF/ IR CAM/ DMIC/ ALS CONN

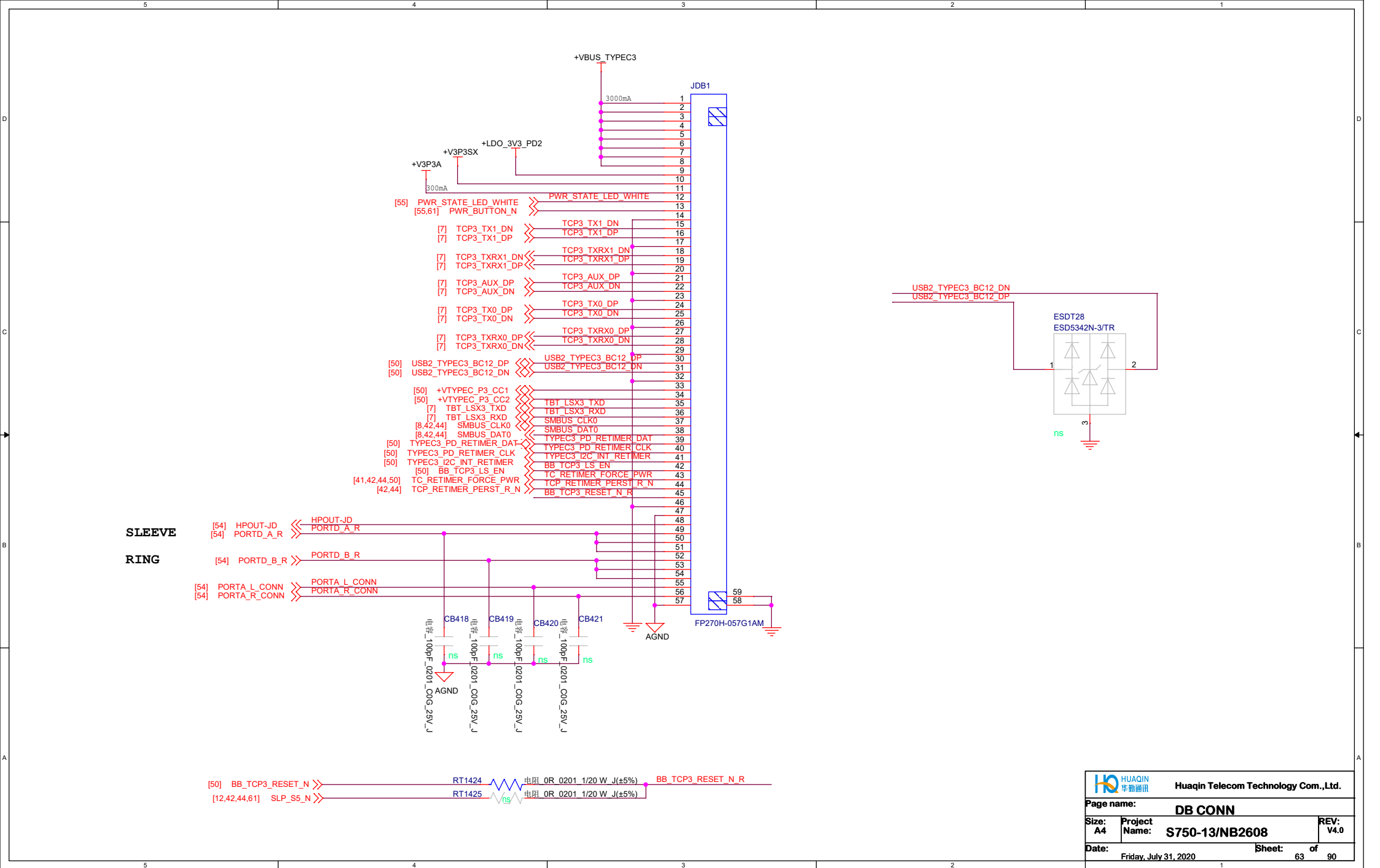


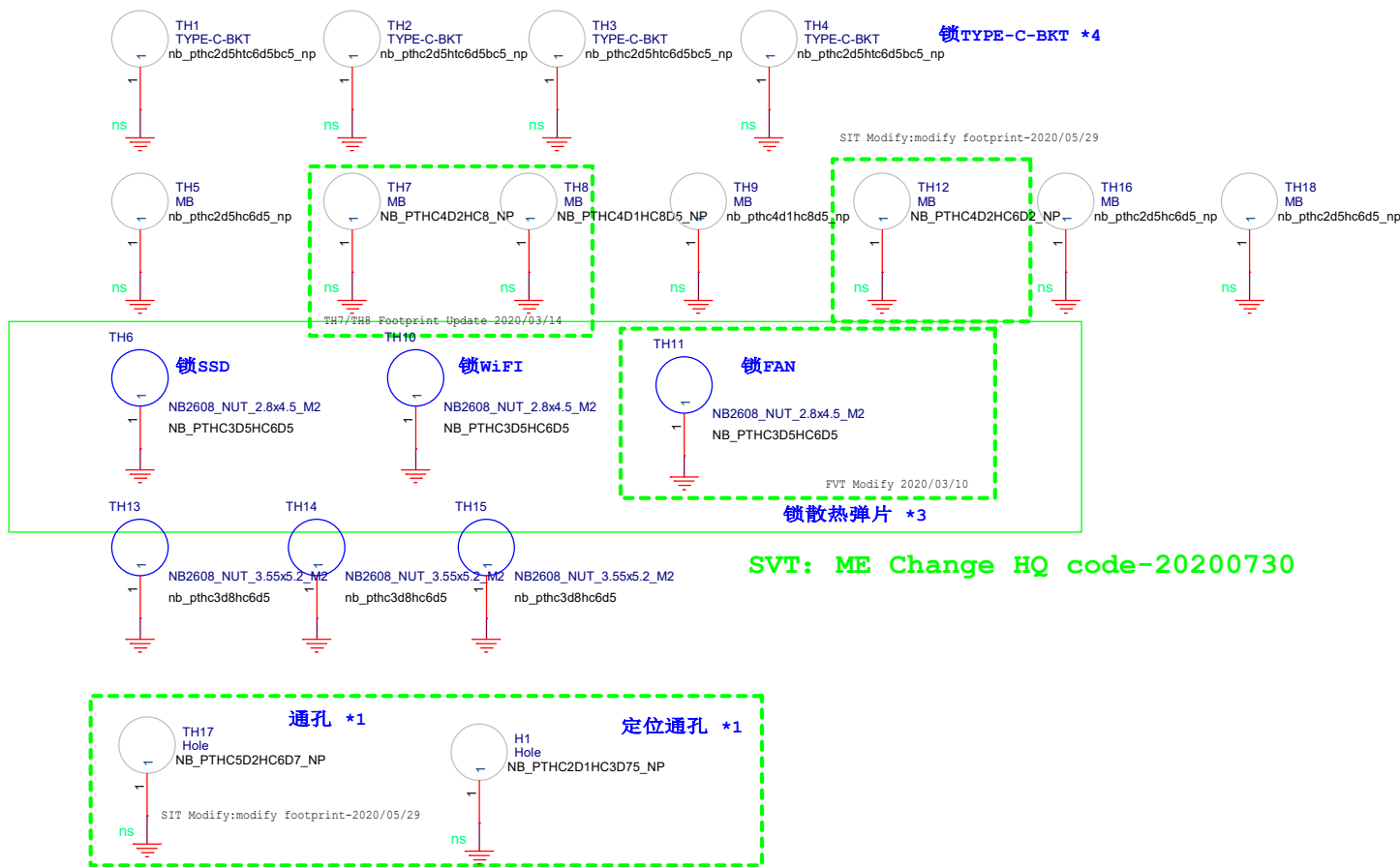
Note: JX2 nb_con30_19d2x5d2x1d95_0d5 Pin1 right

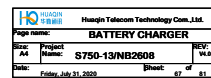


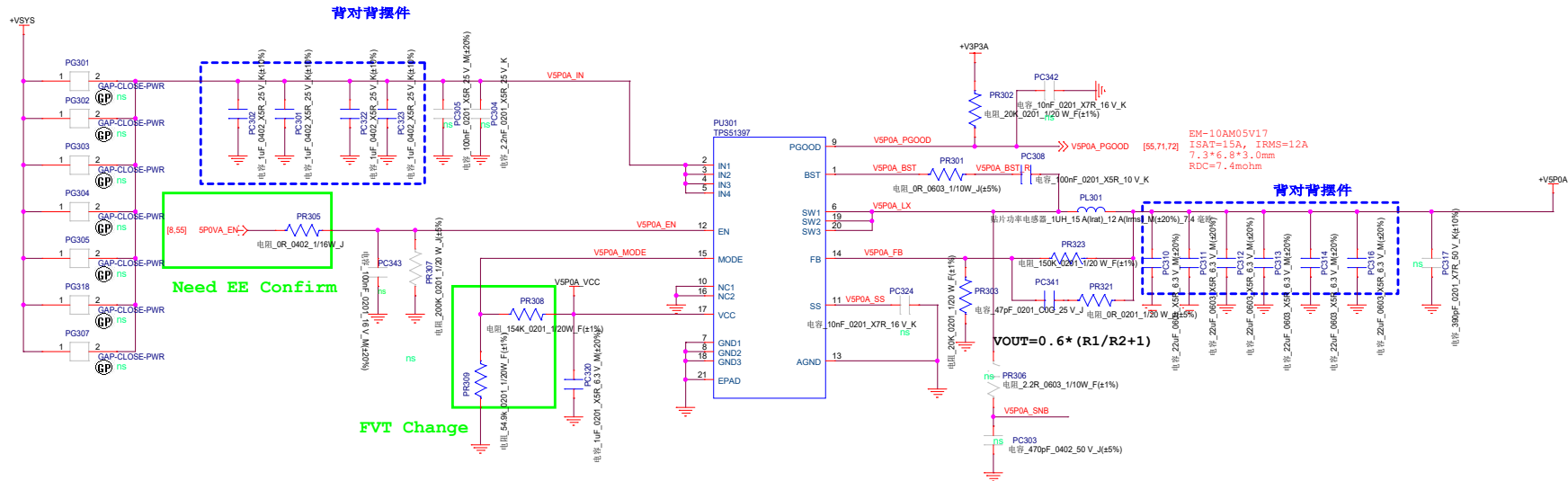
Camera

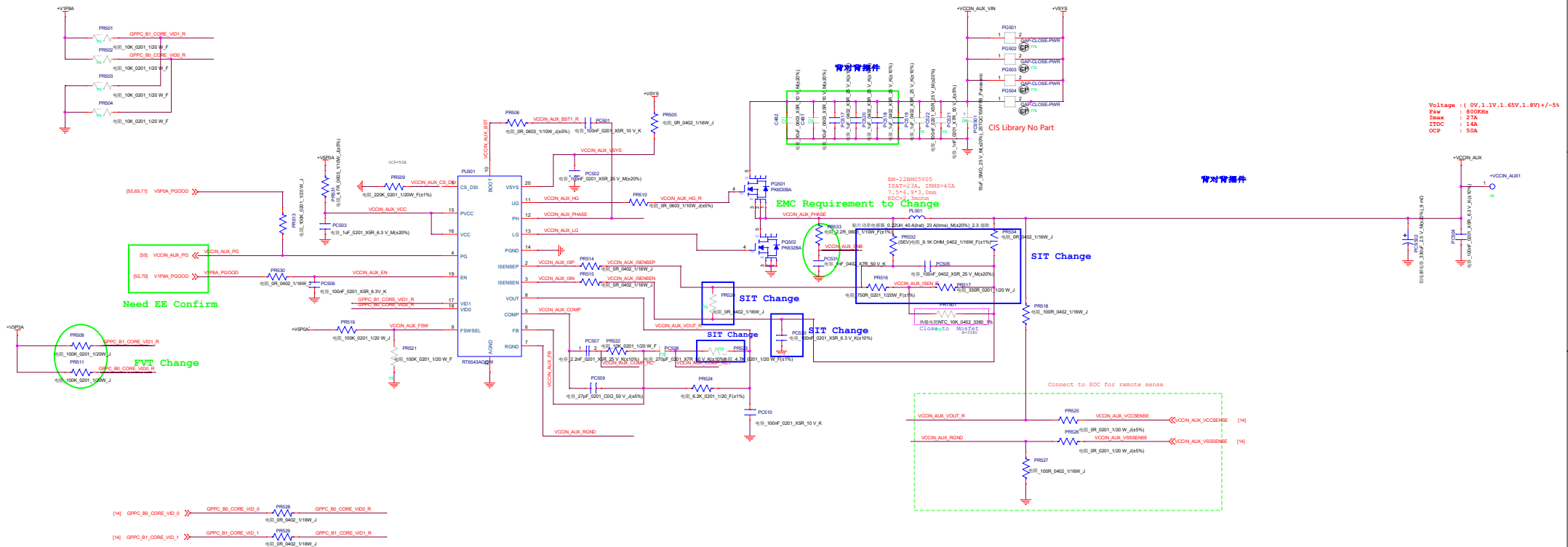


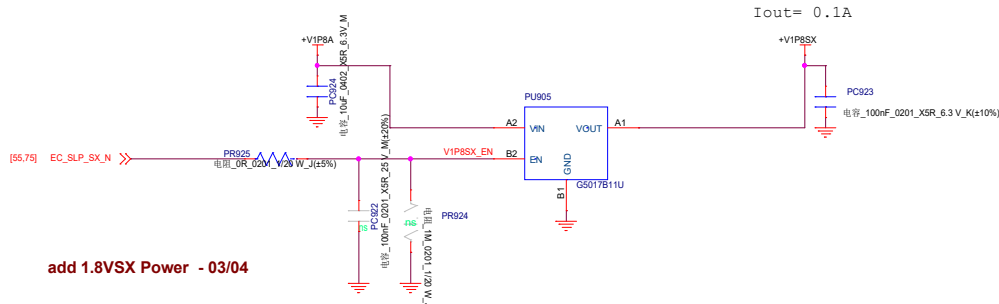




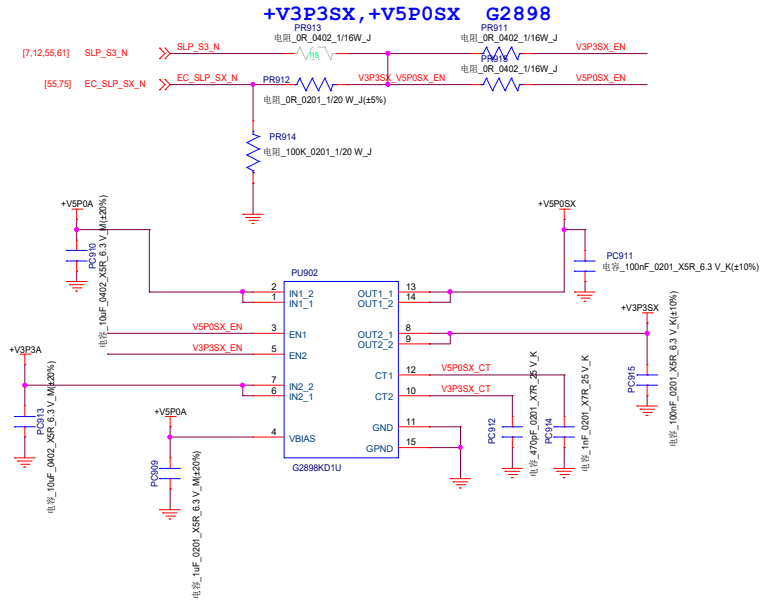
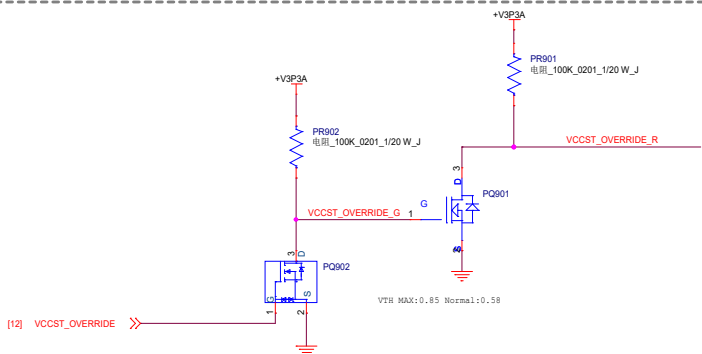




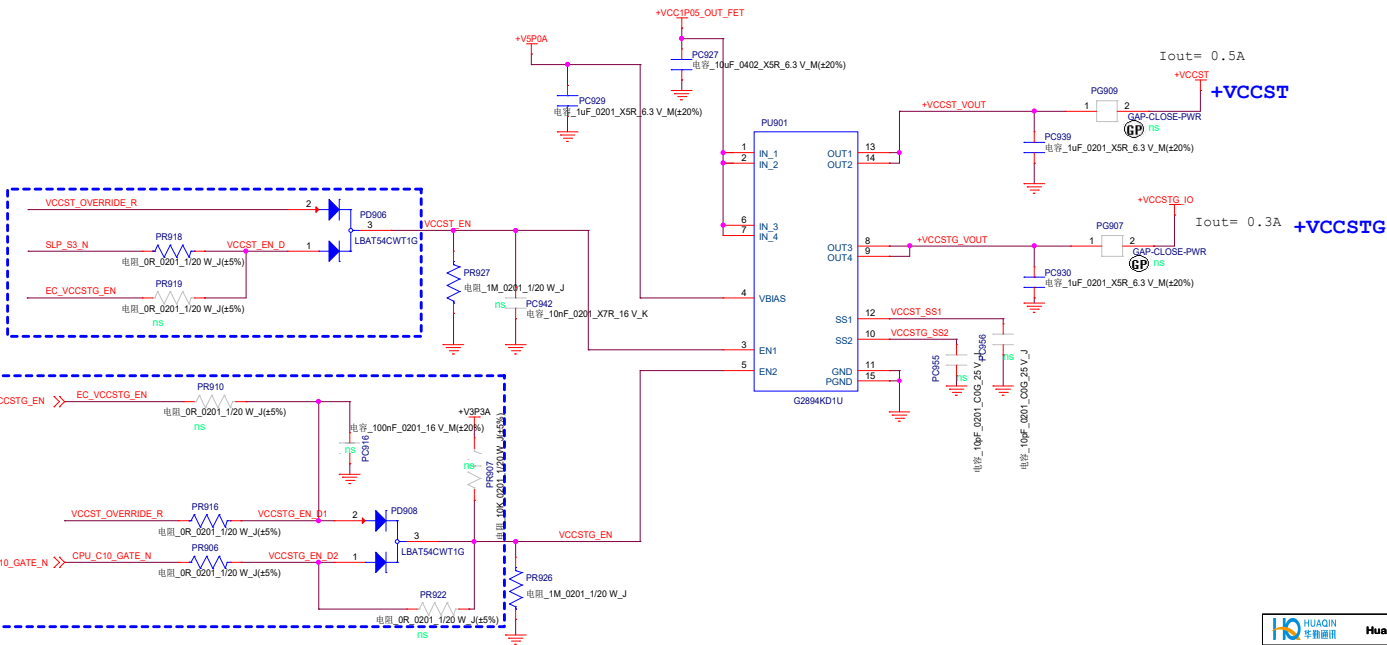




add 1.8V_{VSX} Power - 03/04



+VCCST



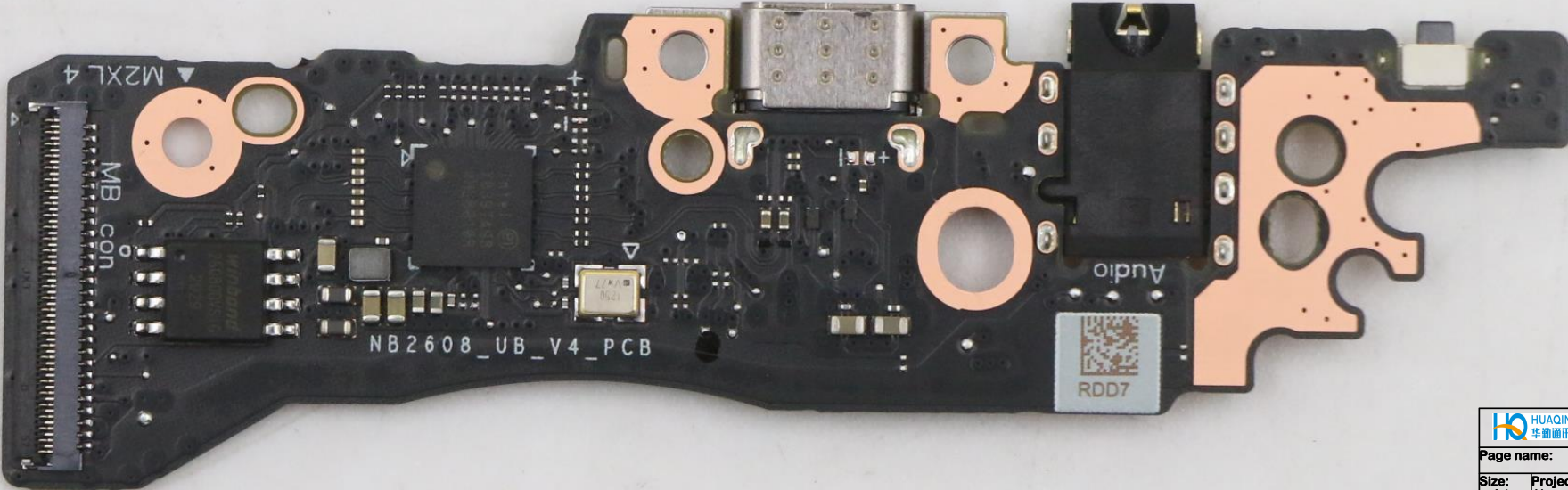
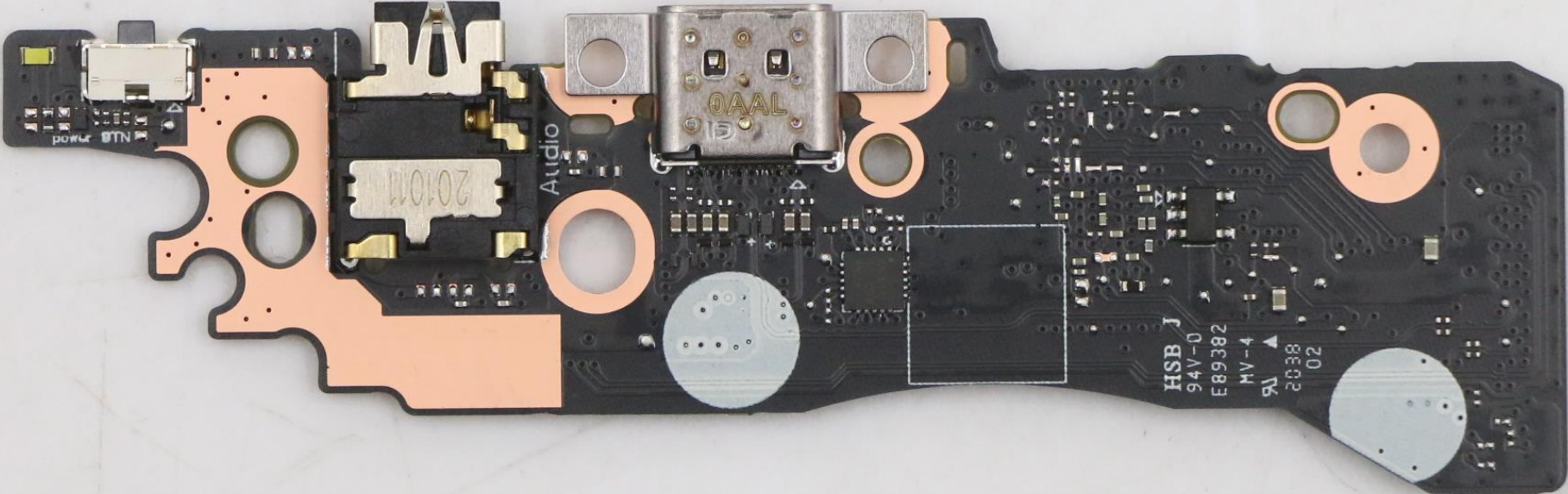
+VCCSTG_IO


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

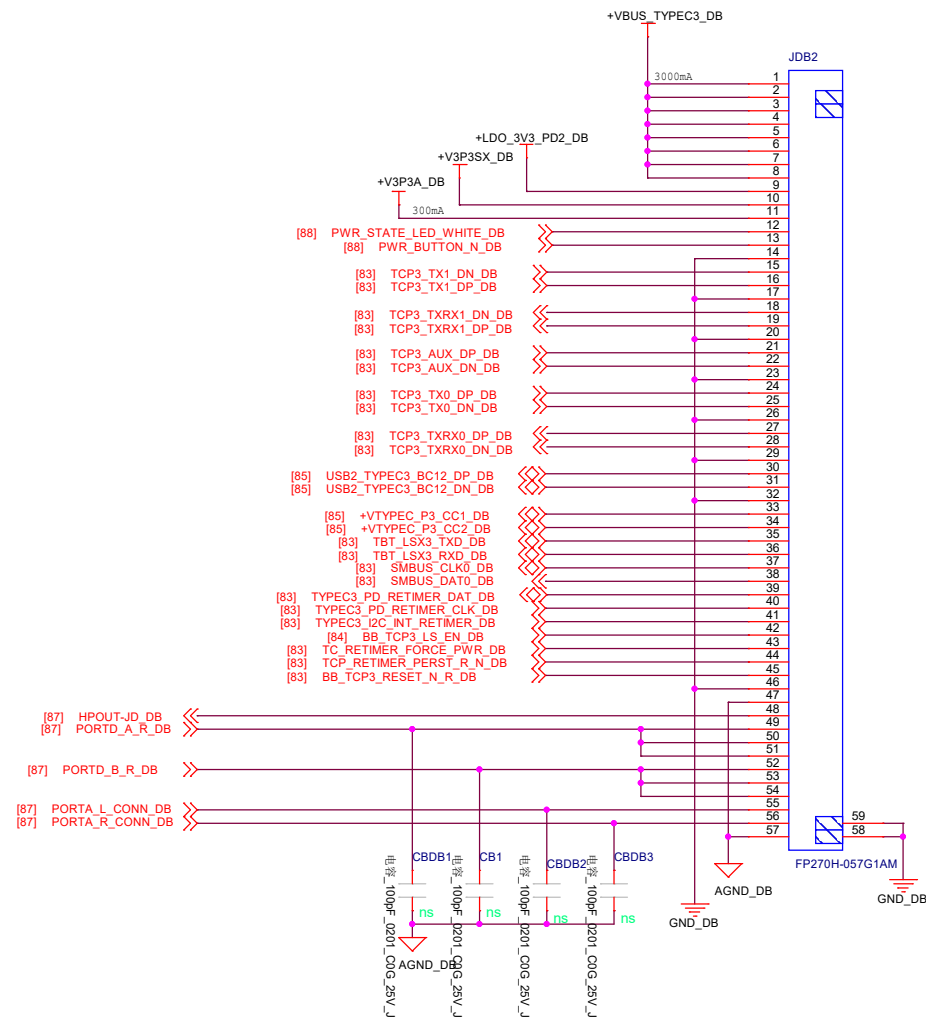
5	4	3	2	1																				
D																								
C																								
B																								
A																								
5	4	3	2	1																				
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Date: Friday, July 31, 2020	Sheet: 79		of	81																				

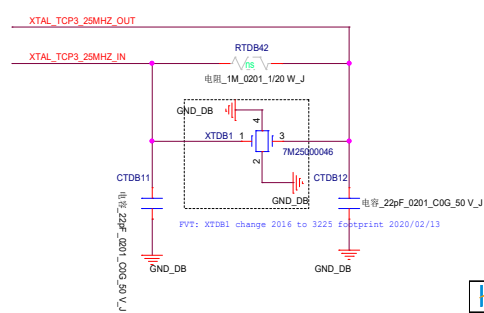
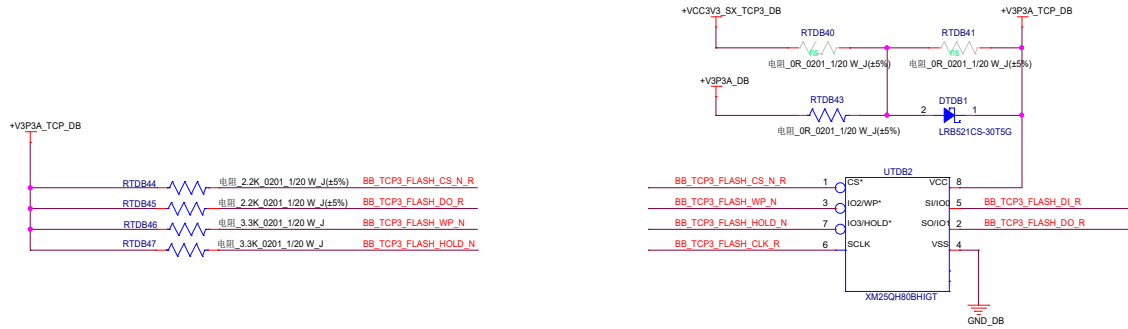
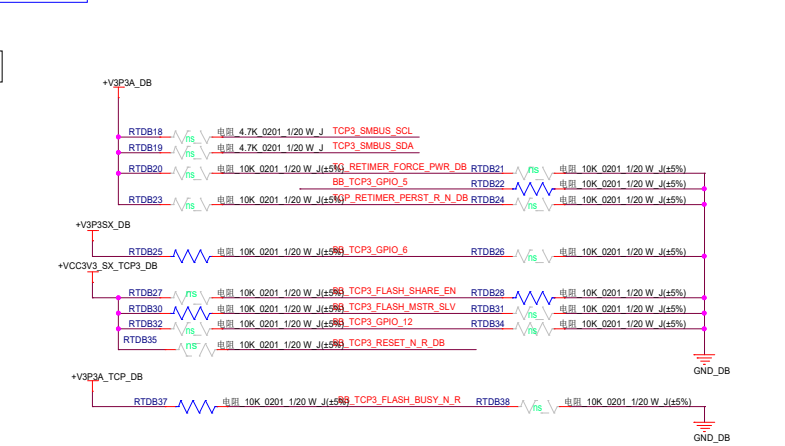
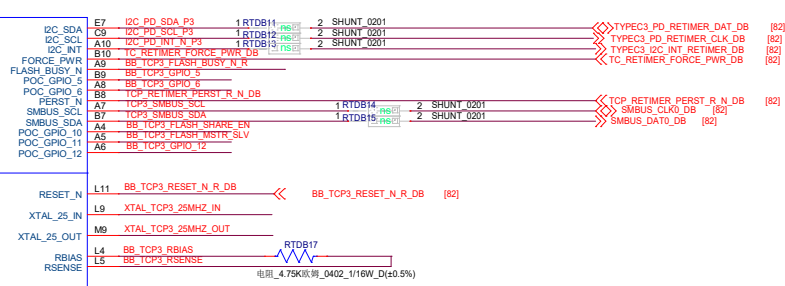
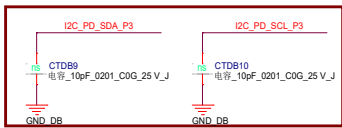
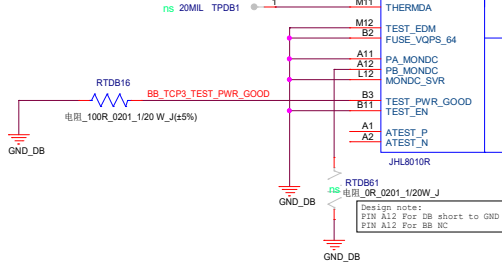
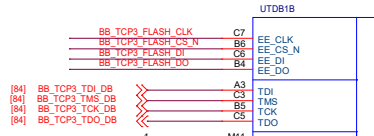
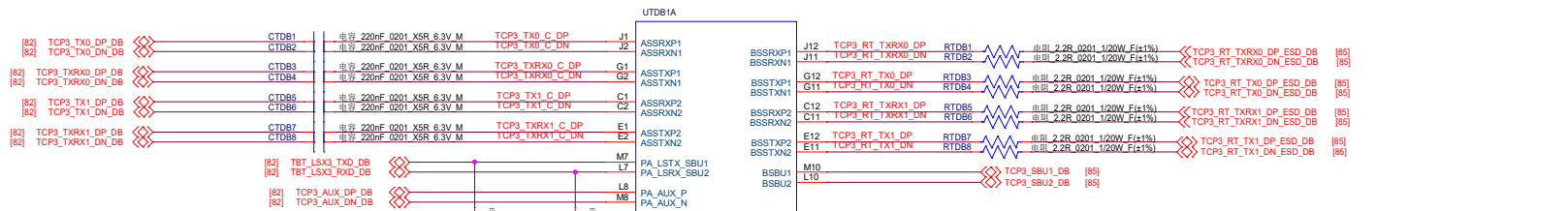
I/O BOARD

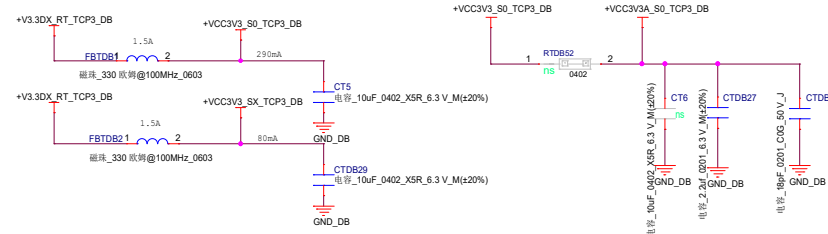
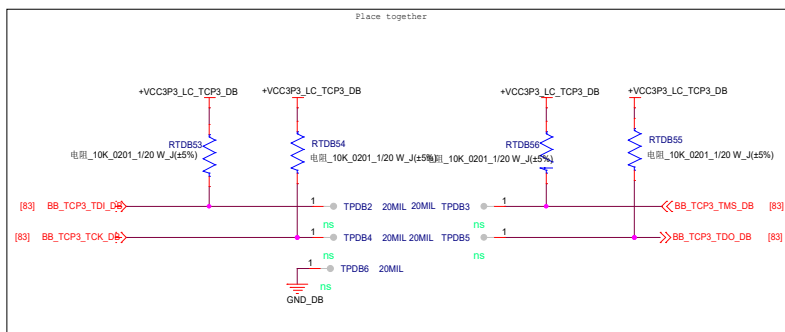
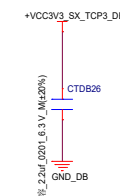
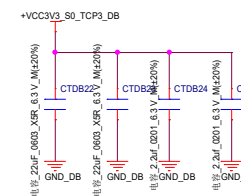
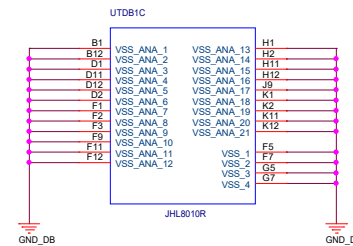
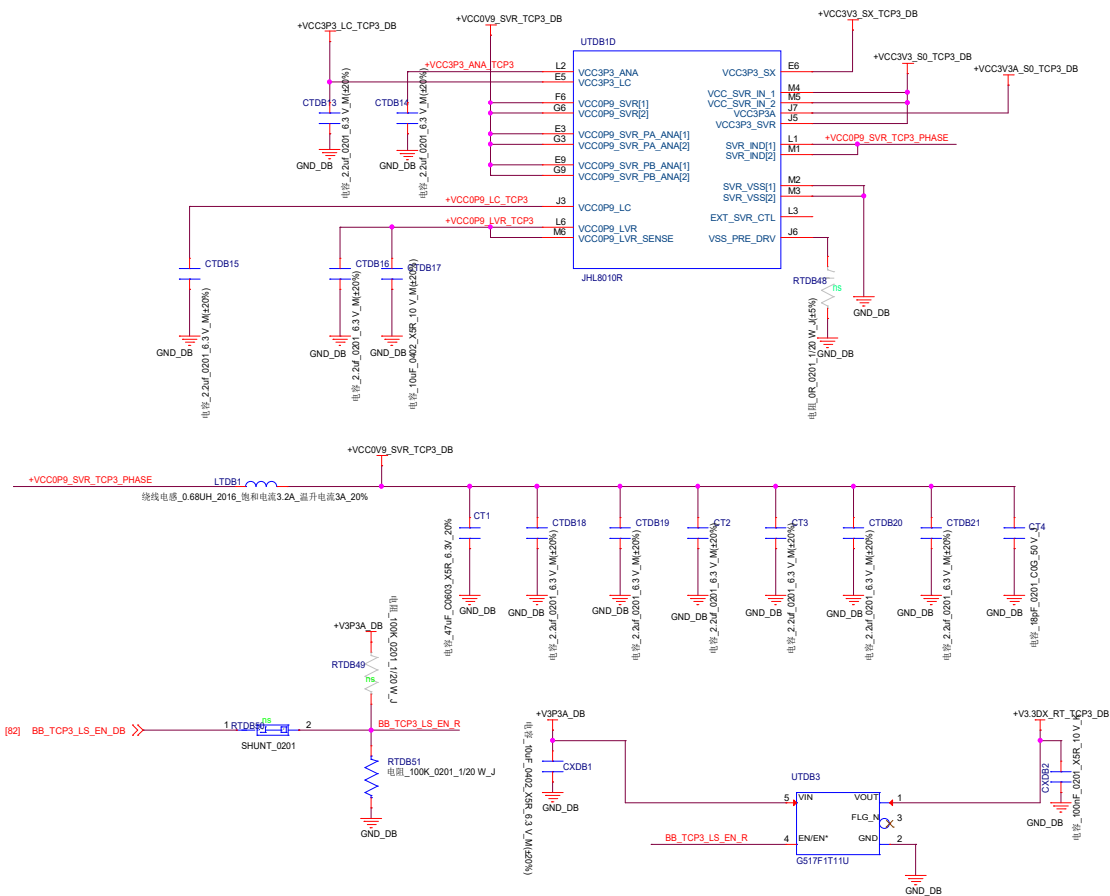


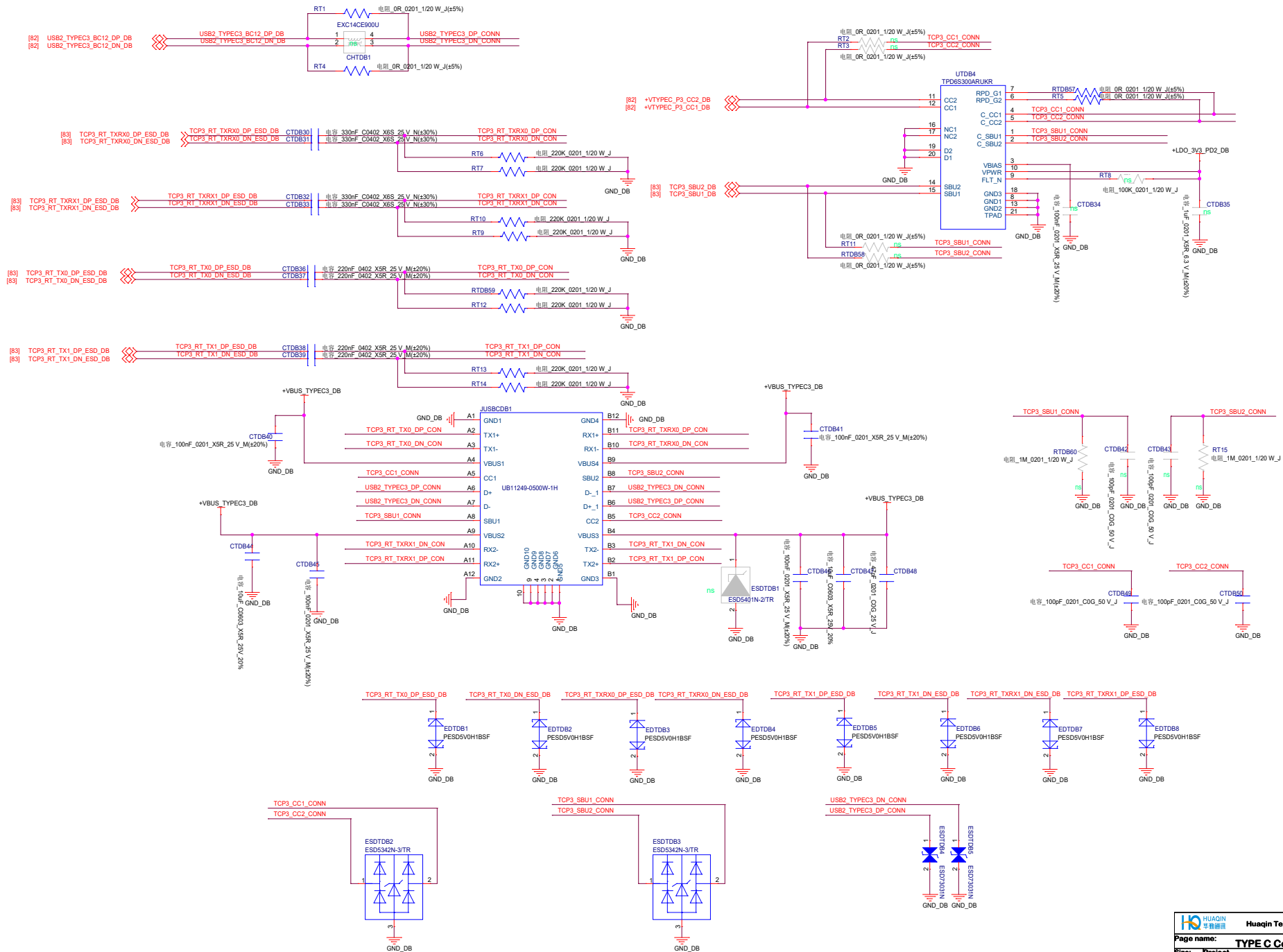
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Size: A4	Project Name: NB2608_UB_V4_PCB	REV: V4.0	
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SLEEVE
RING





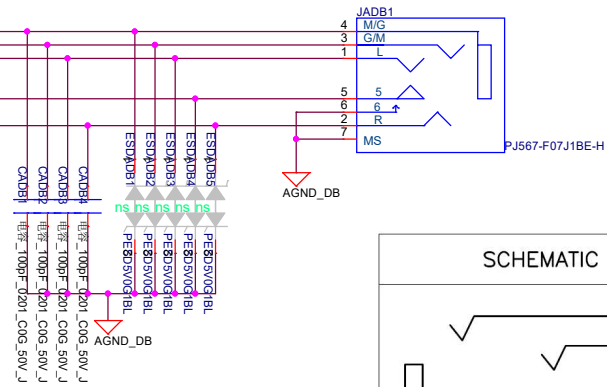




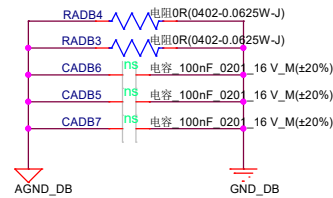
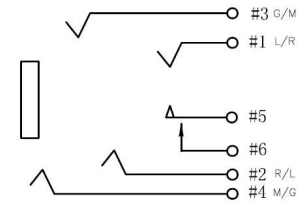
**SLEEVE
RING2**

[82] PORTD_A_R_DB
[82] PORTD_B_R_DB
[82] PORTA_L_CONN_DB

[82] HPOUT-JD_DB
[82] PORTA_R_CONN_DB



SCHEMATIC

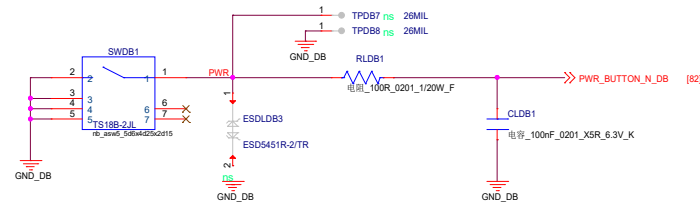


PORTD_A_R_DB	1	●	FTPDB1	26mil	ns
PORTD_B_R_DB	1	●	FTPDB2	26mil	ns
PORTA_L_CONN_DB	1	●	FTPDB3	26mil	ns
HPOUT-JD_DB	1	●	FTPDB4	26mil	ns
PORTA_R_CONN_DB	1	●	FTPDB5	26mil	ns
	1	●	FTPDB6	26mil	ns

AGND_DB

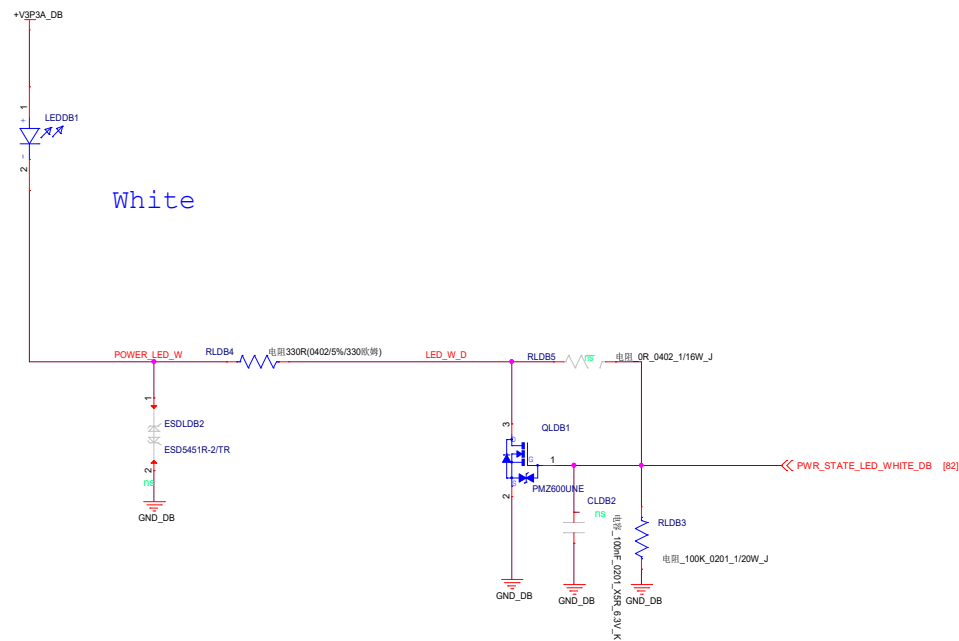
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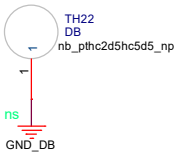
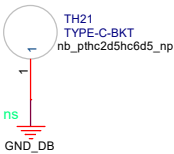
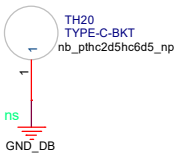
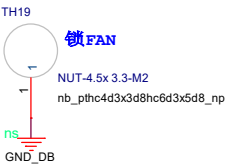
Power BUTTON




Power LED

POWER LED : LEDDB2





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Page name:			
Size: A4		Project Name: S750-13/NB2608	
Date: Friday, July 31, 2020		REV: V4.0	
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90		90	